

Compal Confidential

KBL-Y MB Schematic Document

EPS30 LA-F803P

Rev: 0.3

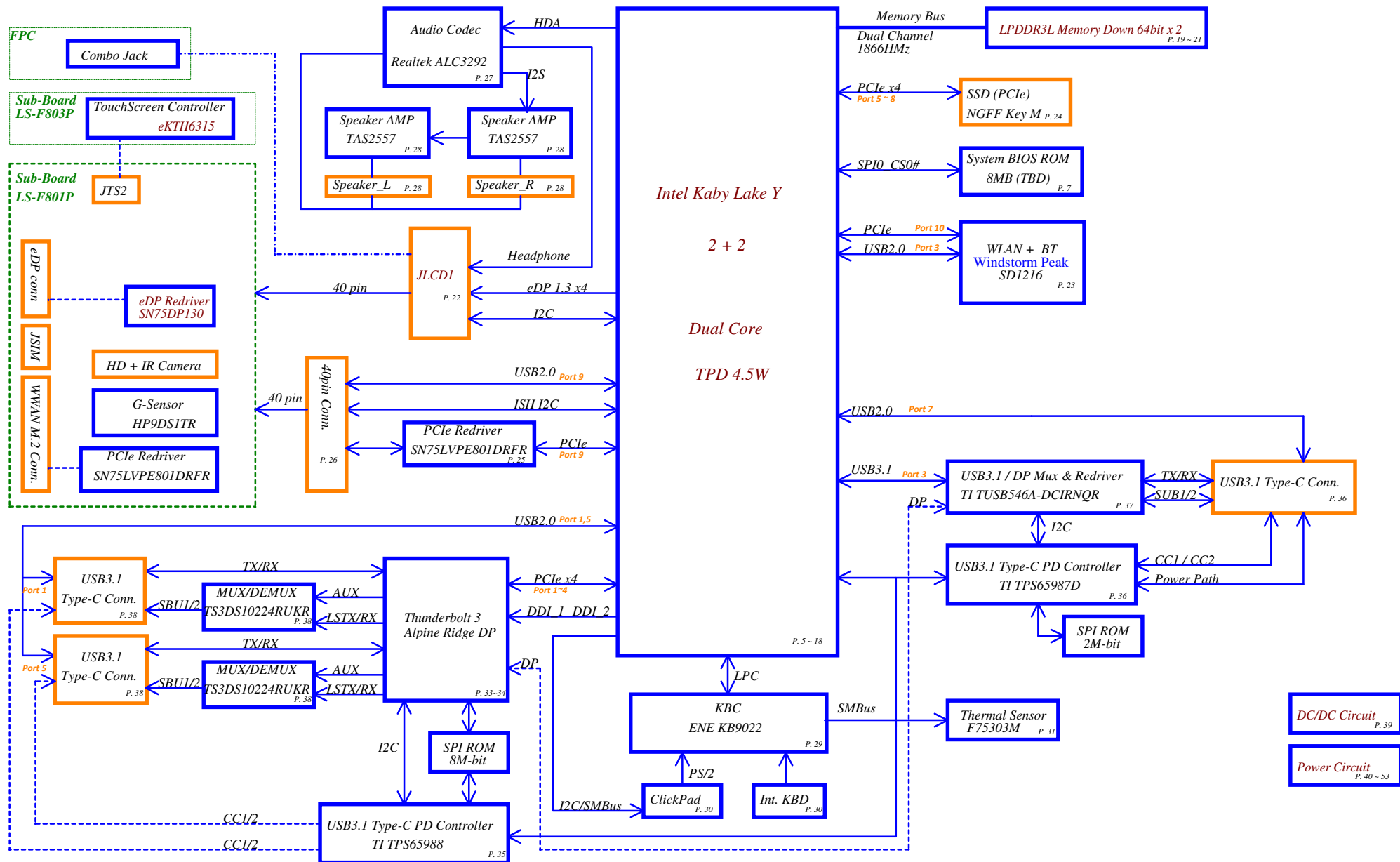
2018.06.08

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					Cover Sheet
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# Kaby Lake Y Block Diagram

(KBL-Y 2+2 w/ LPDDR3L x64, Modern Standby )

Follow Premium Power Segment, S0ix & C10 optimized



V <sub>CC</sub>	3.3V				
R <sub>a</sub>	100K +/- 1%				
Board ID / PCB Revision	R <sub>b</sub>	V <sub>BID</sub> min	V <sub>BID</sub> TYP	V <sub>BID</sub> Max	EC AD3
0 / 0.2	0		0 V	0.300 V	0x00 - 0x0B
1 / 0.3	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
2 / 0.4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x38
4 / 1.0	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54

[illegible]

HSIO Port	Capable	Device	PCIe CLK	NOTE
0	USB3.1 #1			
1	USB3.1 #2			
2	USB3.1 #3	USB3.1 Type-C		USB3.1 Type-C DP with Mux + PD
3	USB3.1 #4			
4	USB3.1 #5 / PCIe #1	Thunderbolt, Alpine Rodge	CLK4 & CLKREQ#4	
5	USB3.1 #6 / PCIe #2			
6	PCIe #3 / GbE			
7	PCIe #4 / GbE			
8	PCIe #5 / GbE	SSD (NGFF_Key M)	CLK2 & CLKREQ#2	PCIe/SATA interface
9	PCIe #6			
10	PCIe #7 / SATA #0			
11	PCIe #8 / SATA #1			
12	PCIe #9 / GbE	WWAN	CLK1 & CLKREQ#1	
13	PCIe #10 / GbE	WLAN	CLK3 & CLKREQ#3	

SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Number	Load BOM Option
431ACZ32L01	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Mi@/R1I7@
431ACZ32L02	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Hy@/R1I5@
431ACZ32L03	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Mi16@/R1I7@
431ACZ32L04	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Sam@/R1I5@
431ACZ32L05	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Mi16@/R1I7R@
431ACZ32L06	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Mi16@/R1I5R@
431ACZ32L07	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Hy@/R1I7R@
431ACZ32L08	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Mi@/R1I5R@
431ACZ32L09	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Sam@/R1I7R@
431ACZ32L10	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Hy@/R1I5R@
431ACZ32L11	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Mi@/R1I7R@
431ACZ32L12	@CPUPWM@/LPC@/MP@/SOIX@/X4E@/RF@/R1Sam@/R1I5R@

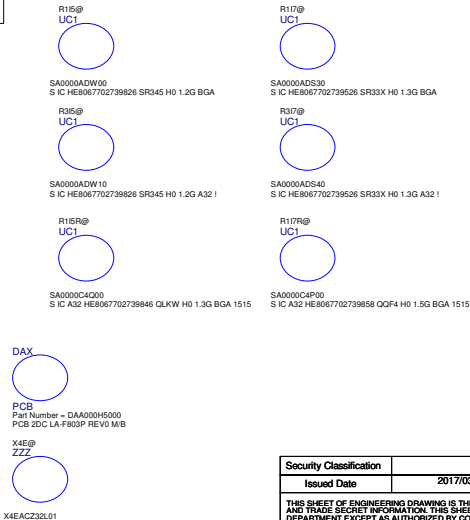
USB2.0 Port	Device	NOTE
1	USB2.0 (MB)	USB3.1 Type-C + PD
5	USB2.0 (MB)	USB3.1 Type-C + PD
7	USB2.0 (MB)	USB3.1 Type-C + PD
3	Blue Tooth	WLAN 8265
9	IR Camera	
2,0	X	

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SOC_SMBCLK SOC_SMBDATA	+3V_PRIM	Track PAD	TBC	TBC	TBC
SOC_SML0CLK SOC_SML0DATA	+3VS	N/A	N/A	N/A	N/A
SML1_SMBCLK SML1_SMBDAT	+3VS	EC	TBC	TBC	TBC

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBUS Port 1	+3V_SMBUS	BATT	0x0B	0x16	0x17
		Charger	0x09	0x12	0x13
SMBUS Port 2	+3VL_EC	TPS65988(1)	0x25	TBC	TBC
		TPS65988(2)	0x21	TBC	TBC
		TPS65987D	0x23	TBC	TBC
		F75303M	1001_101xb		
		Power CHIP	TBC	TBC	TBC
SMBUS Port 3	+3VALW	SN75DP130			
		Codec	TBC	TBC	TBC
		SPK AMP	TBC	TBC	TBC

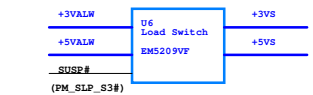
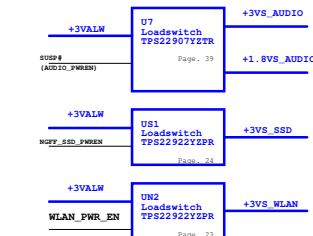
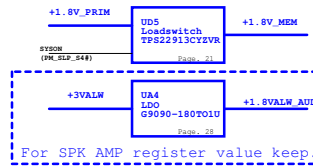
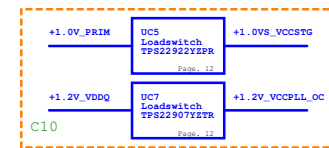
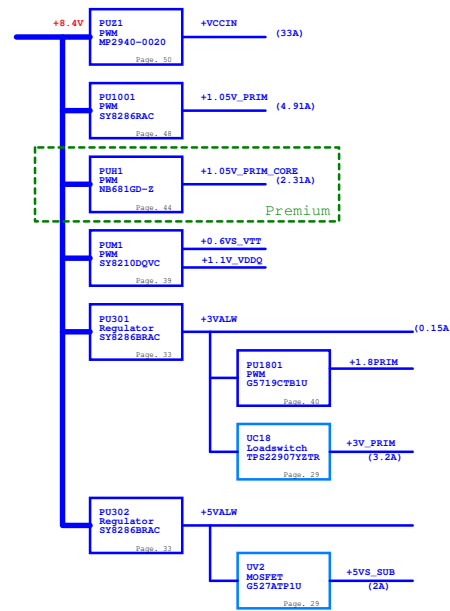
I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C 0	+3VS	Track PAD(Reserved)	0x2C	TBC	TBC
I2C 1	+3V_PRIM	Touch Screen	0x10b	TBC	TBC
ISH_I2C 0	+3VALW	HP9DS1TR	1101011xb 0011110xb	TBC	TBC

Power plane / State	+3VALW_DSW +3VALW +3VALW +13VALW +13VALW +3VLP	+3V_PCH +3V_PCH +3V_PCH +13V_GATE +VCC_PCH	+12V_DDR +33V_OEM +33V_OEM +13V_VCCST +13V_VCCST	+5VS +5VS +5VS +5VS_VCCST +5VS_VCCST +5VS_VTT +5VS_VTT +5VS_VTT +5VS_VTT +VCC_CORE
S0	ON	ON	ON	ON
S3 /AC	ON	ON	ON	OFF
DS3	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF



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## [EPS30-SMBus Map]



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## Functional Strap Definitions

GPP\_E19 (Internal Pull Down): DDPB\_CTRLDATA

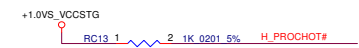
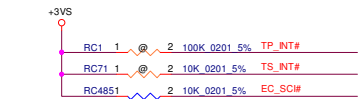
0 = Port B is not detected.

1 = Port B is detected.

GPP\_E21 (Internal Pull Down): DDPC\_CTRLDATA

0 = Port C is not detected.

1 = Port C is detected.



PV: HPD double pull down

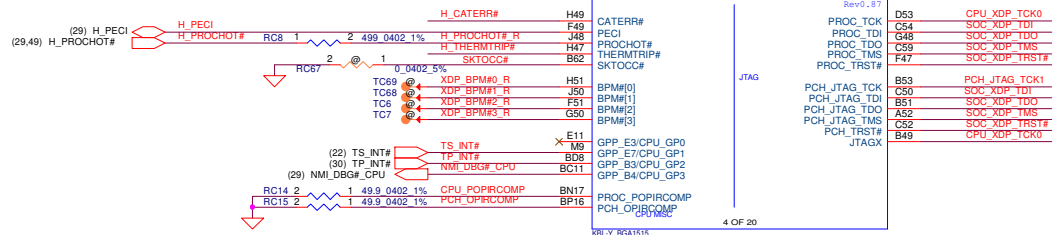
Alpine Ridge

+0.85VS\_VCCIO



RC4 Width 20 mils, Spacing 25 mils,  
Length < 100 mil

PV: delete TS\_RST#\_PCH  
RC4 2 49.9 0402 1%  
RC4 2 49.9 0402 1%  
RC4 2 49.9 0402 1%

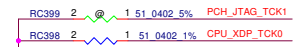
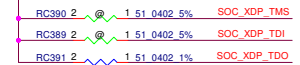


PDG\_Processor strap CFG[4] should be pulled low to enable embedded DisplayPort\*

<eDP>

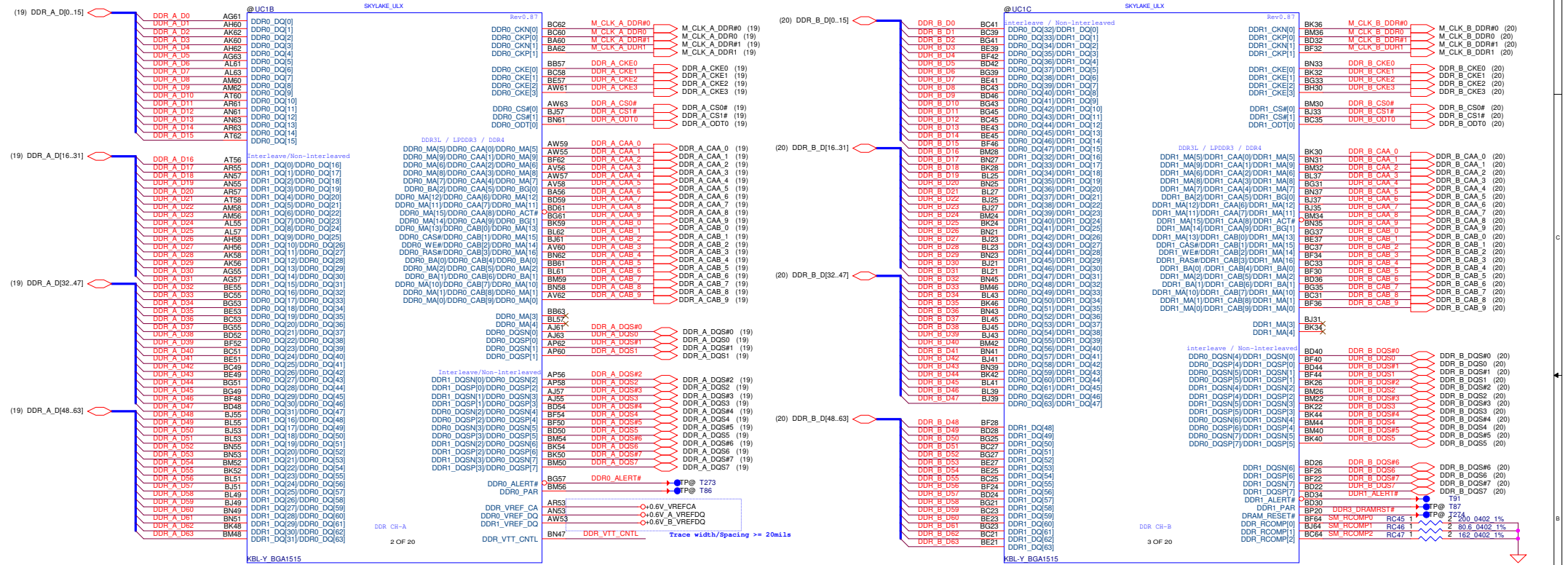
TBT

+1.0VS\_VCCSTG Place to CPU side

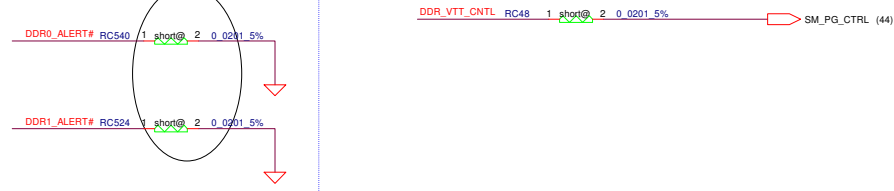


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# Non-Interleave Memory



Reserve



2016-08-24  
Modify-Follow TD team

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Issued Date	2041/09/08	Deciphered Date	2013/10/28	SKL Y2(1/3) DDRIII
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## Functional Strap Definitions

### GPP\_C2 (Internal Pull Down): SMBALERT#

0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).

1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

Connect TP

PV: modify for RTD3

## Functional Strap Definitions

### GPP\_C5 (Internal Pull Down): SML0ALERT#

0 = LPC is selected for EC.

1 = eSPI is selected for EC.

### GPP\_B23..SML1ALERT#

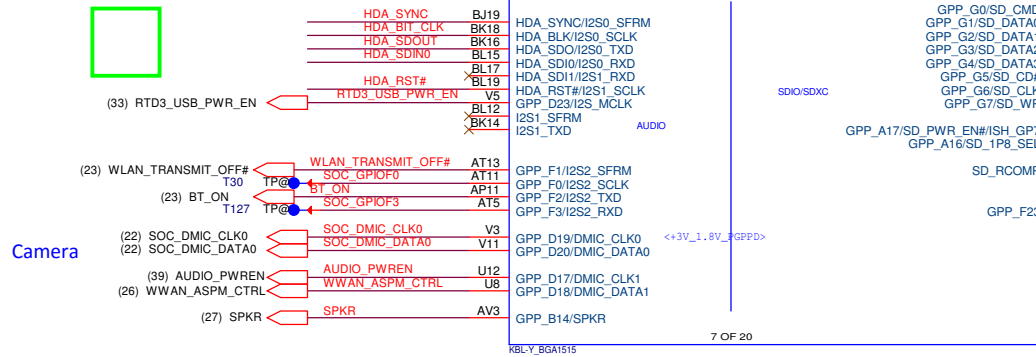
• If USB 3.0 Port 1 is used for DCI.00B (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.

• If USB 3.0 Port 1 is used for DCI.00B (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float.

• If DCI.00B (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.

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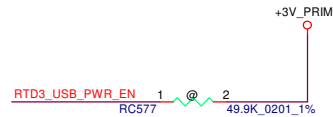
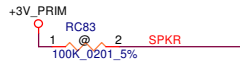
A00\_0906: EMI Request RH109 33chnage 56ohm



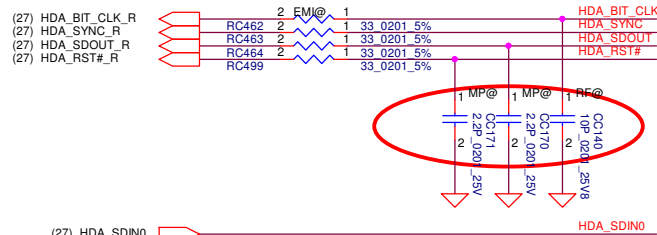
561280\_KBL UY PDG Rev2\_0  
if SDXC interface is not used,  
the SD\_RCOMP pin does not need to be connected to a RCOMP resistor.

## Functional Strap Definitions

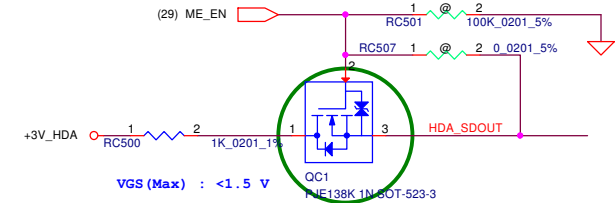
GPP\_B14 (Internal Pull Down): SPKR  
TOP Swap Override  
0 = Disable TOP Swap mode.----> AAU30 Use  
1 = Enable TOP Swap Mode.



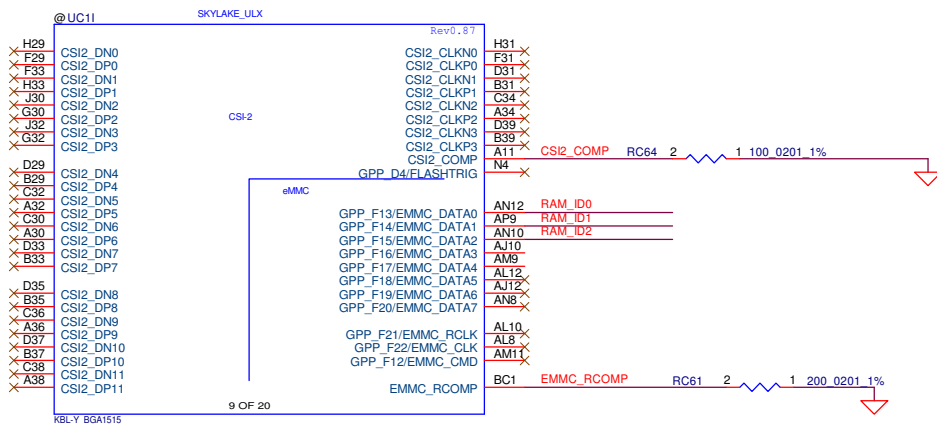
## HDA for AUDIO



## To Enable ME Override

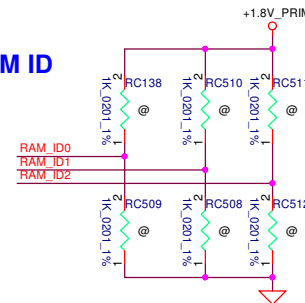


HDA\_SDO / I2S0\_TXD (Internal Pull Down)(Primary well):  
Flash Descriptor Security Override  
0 = Enable (Default)  
1 = Disable (Override)  
The internal pull-down is disabled after PCH\_PWROK is High.



## DDR Memory Configuratio Type Strap pin

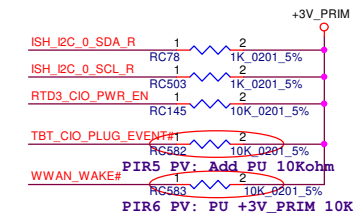
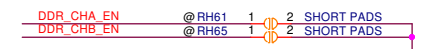
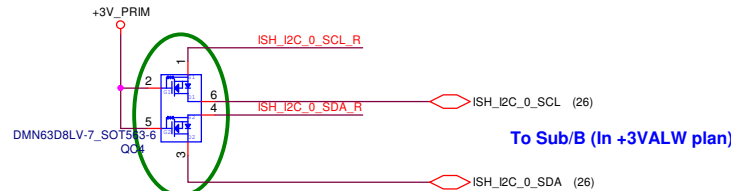
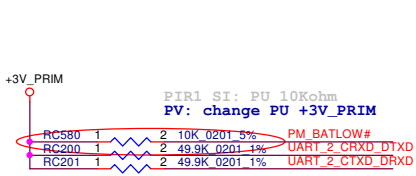
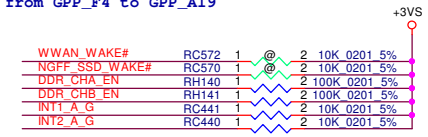
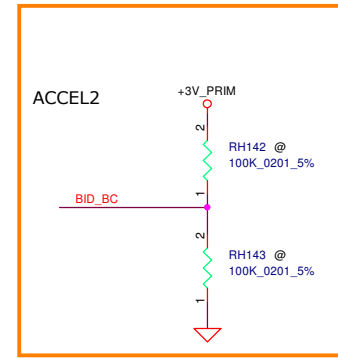
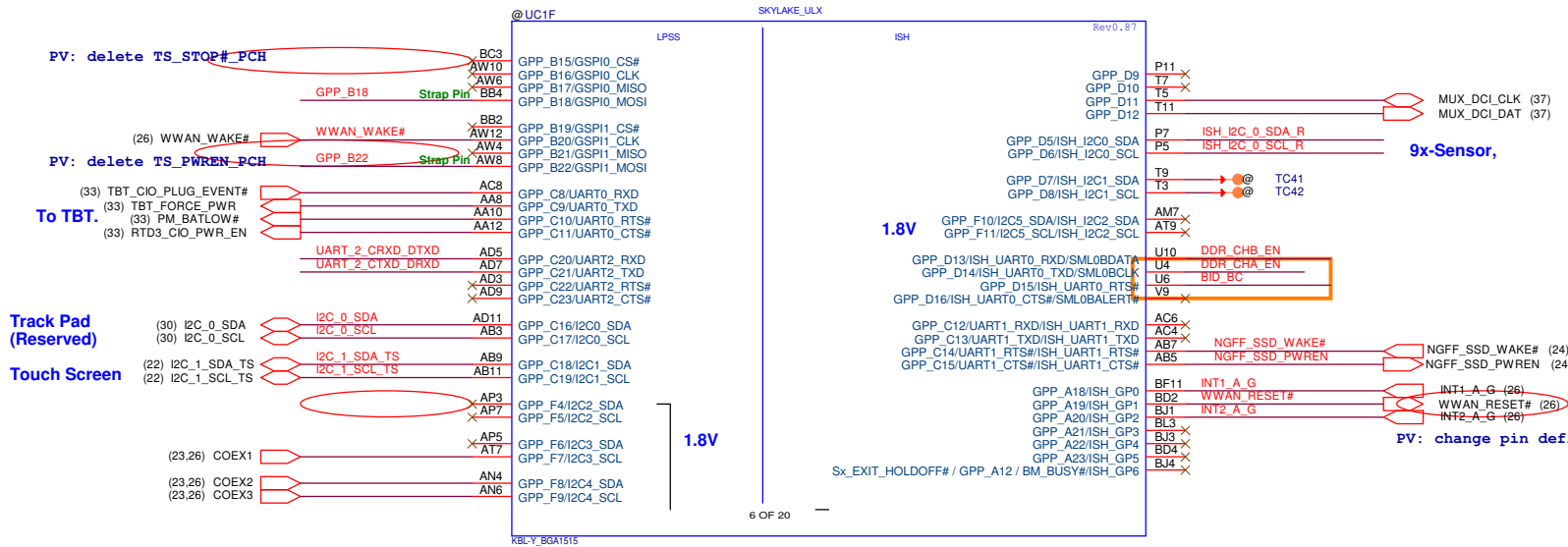
### RAM ID



SKU	RAM_ID2/1/0	Config	P/N	Description	Matched Resister
L01	000	Micron 8G LPDDR3L	R1 SA000092800	S IC D3 512M64 MT52L512M64D4PQ-107WT:B FBGA	RC509 RC508 RC512
L02	001	Hynix 8G LPDDR3L	R1 SA000092J20	S IC D3 32G/1866 H9CCNNCPTALBR-NUD FBGA	RC138 RC508 RC512
L04	010	SAMSUNG 8GB LPDDR3L	R1 SA00009DC00	S IC D3 32G/1866 K3QF4F40BM-AGCF FBGA	RC509 RC510 RC512
L03	011	Micron 16G LPDDR3L	R1 SA0000C1800	S IC D3 64G/1866 MT52L1G64D8QC-107 WT:B FBGA	RC138 RC510 RC512
		Micron 8GB LPDDR3L	R3 SA000092810	S IC D3 MT52L512M64D4PQ-107WT:B A32!	
		Hynix 4GB LPDDR3L	R3 SA000092J30	S IC D3 32G/1866 H9CCNNCPTALBR-NUD FBGA A32 !	
		SAMSUNG 4GB LPDDR3L	R3 SA00009DC10	S IC D3 32G/1866 K3QF4F40BM-AGCF A32 !	

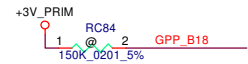
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						Size		Document Number		Rev	
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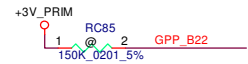
### Functional Strap Definitions

**GPP\_B18 (Internal Pull Down):** GSSPIO\_MOSI  
**No Reboot**  
0 = Disable No Reboot mode. --> AAU30 Use  
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



### Functional Strap Definitions

**GPP\_B22 (Internal Pull Down):** GSSPI1\_MOSI  
**Boot BIOS Strap Bit**  
0 = SPI Mode --> AAU30 Use  
1 = LPC Mode

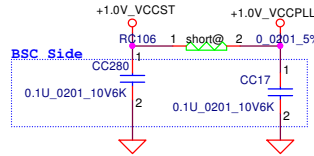


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Issued Date	2041/09/08	Deciphered Date	2013/10/28	SKL Y(6/13) GPIO,LPIO,I2C	
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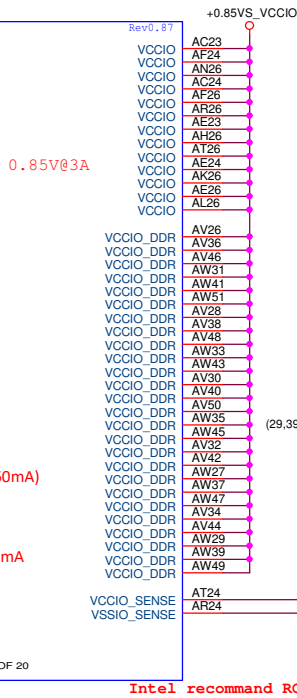
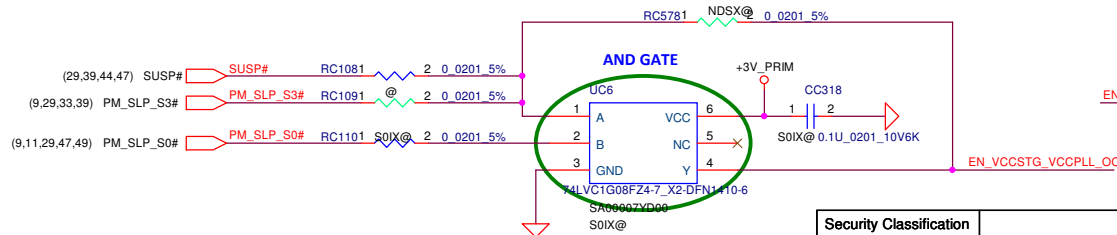
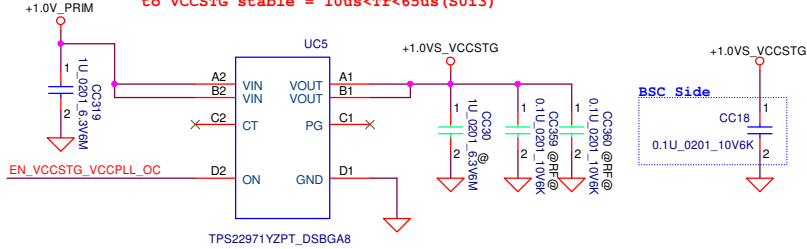
VDDQC trace  
filter width = 6mm  
Total etch length  
= 186.94mils  
PDG P597

VCCST : Sustain voltage for processor standby  
modes  
VCCSTG : Gated sustain voltage for processor standby  
modes



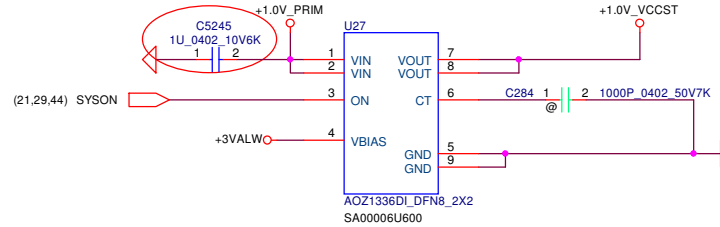
### +1.0V\_PRIM TO +1.0VS\_VCCSTG

tCPU26:CPU\_C10\_GATE# de-assertion  
to VCCSTG stable = 10us<Tr<65us(S0i3)

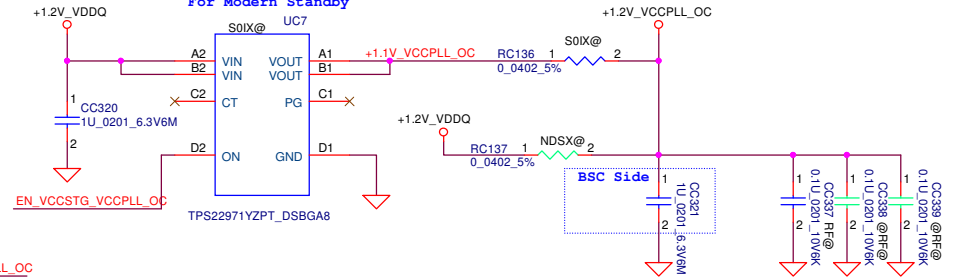


Intel recommend RON(Max) : 70m ohm

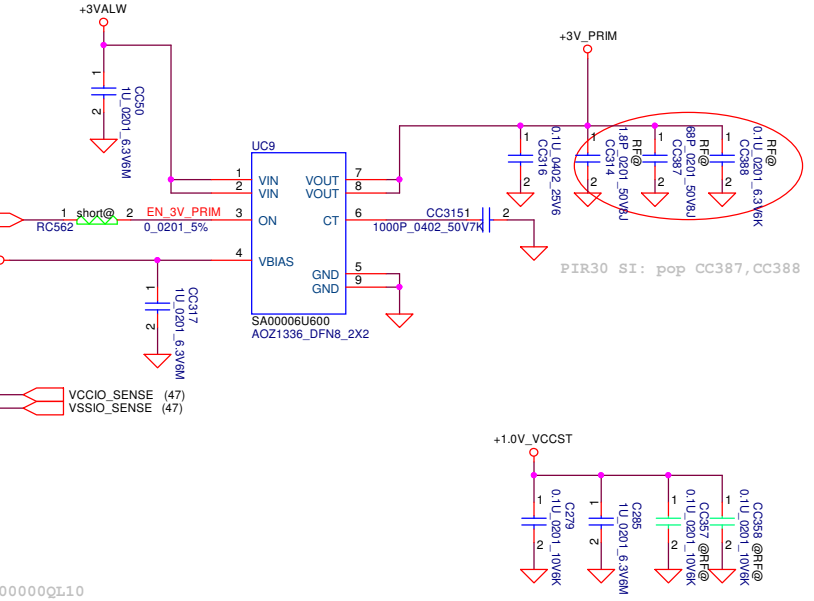
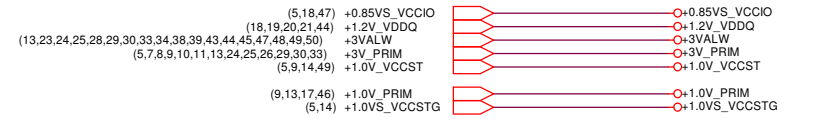
PIR8 SI: From SE000000K80 to SE000000QL10



For Modern Standby

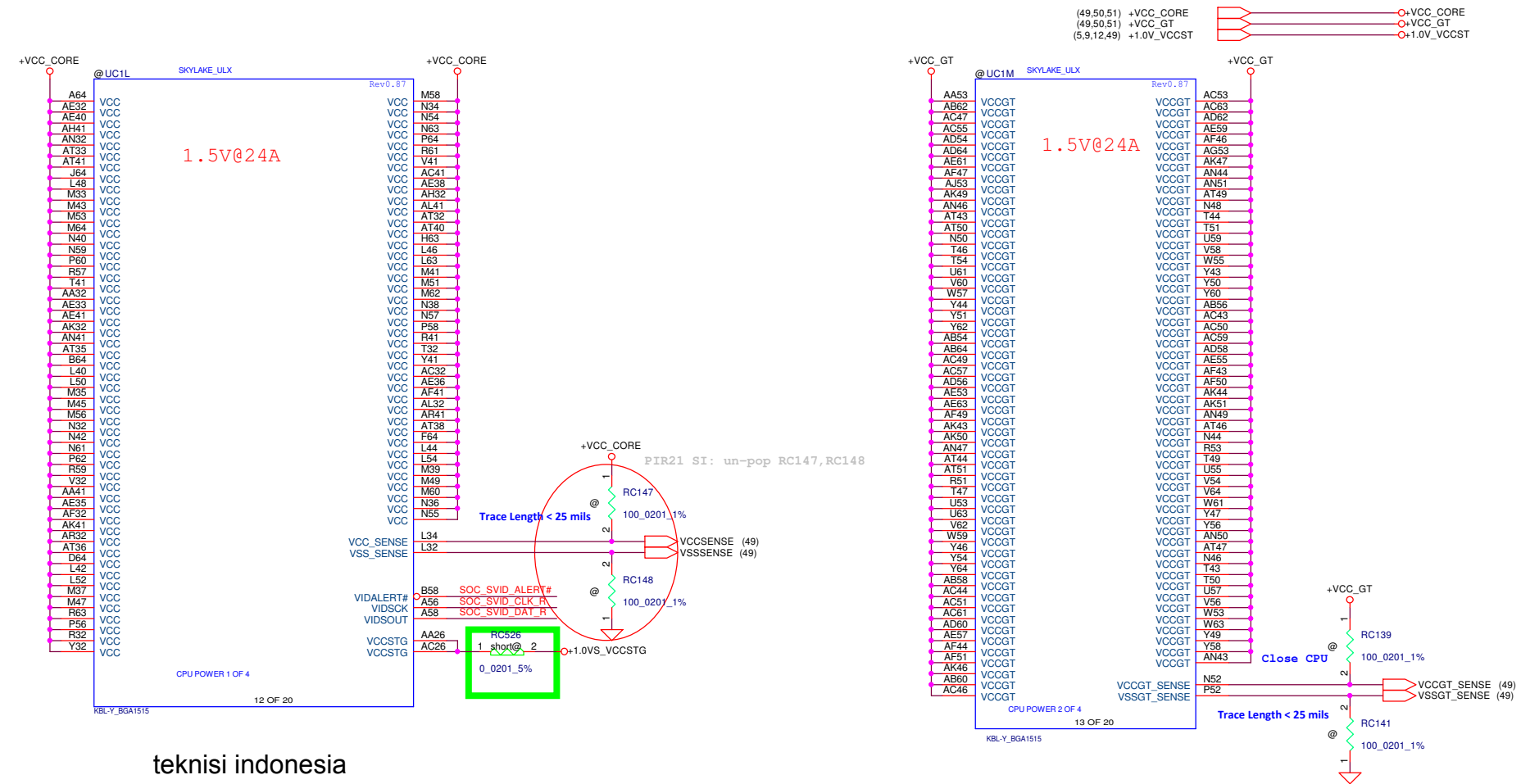


### +3VALW TO +3V\_PRIM

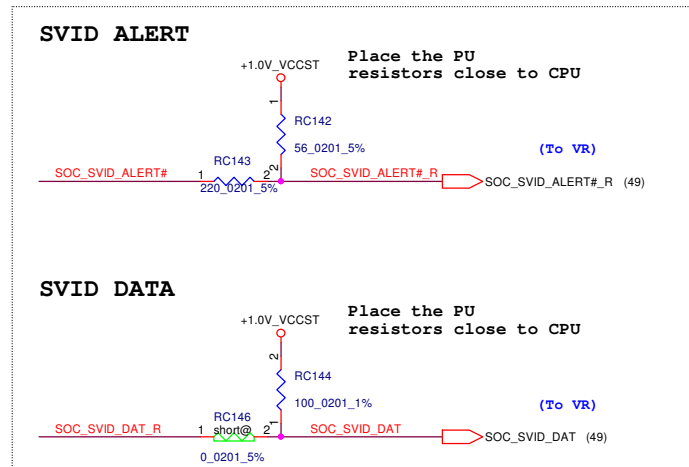


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teknisi indonesia

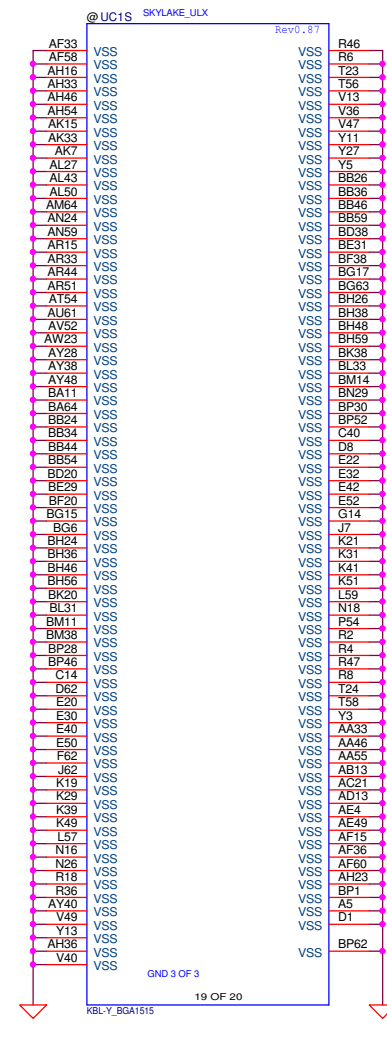
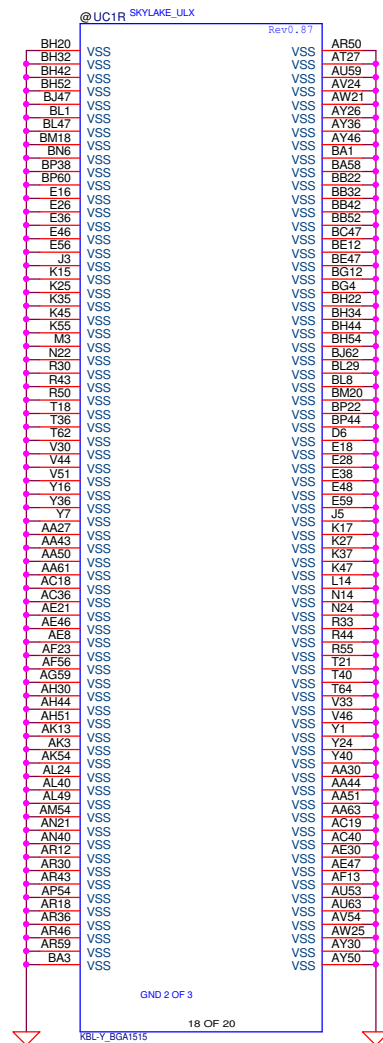
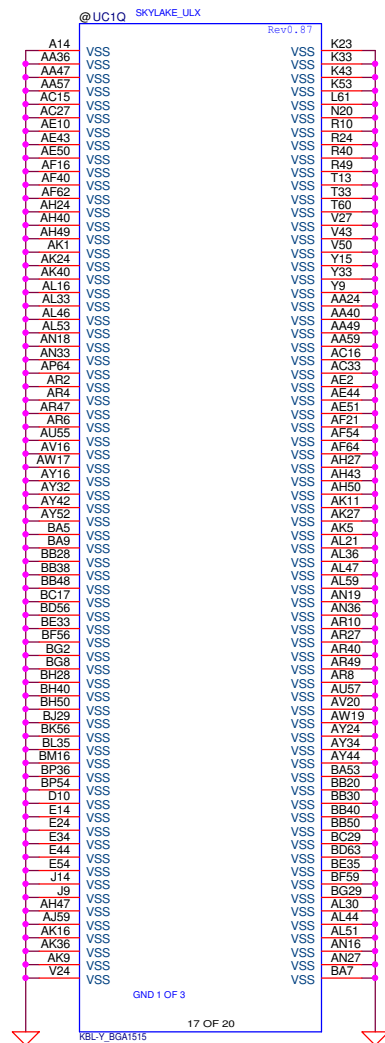


SVID CLK



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						Size		Document Number		Rev	
						LA-F803P		0.1			
						Date:		Friday, June 08, 2018		Sheet 14 of 55	



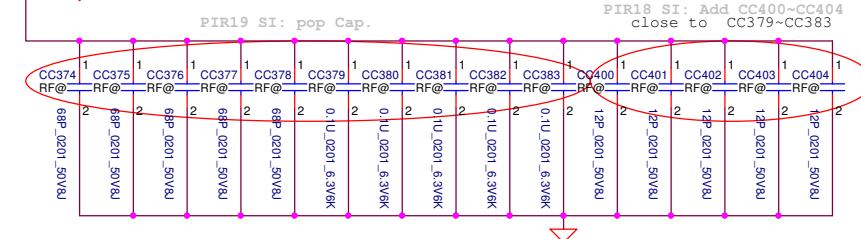
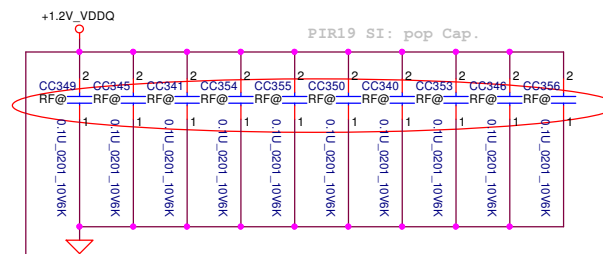
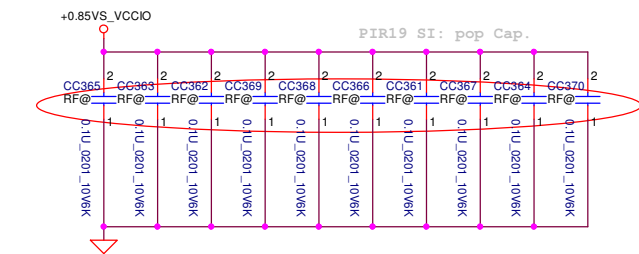
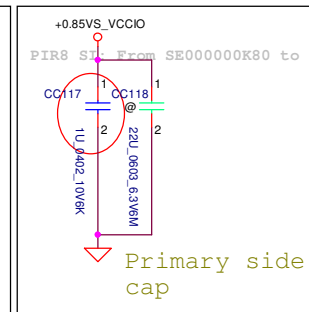
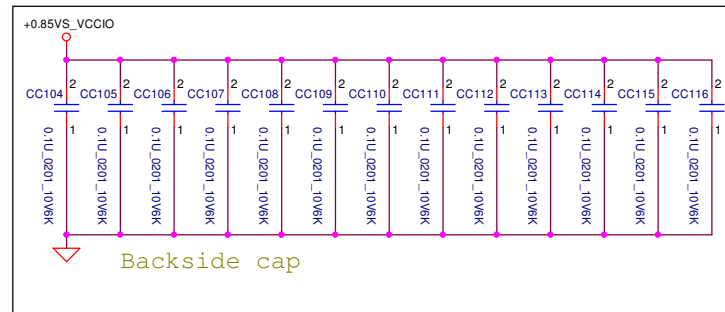
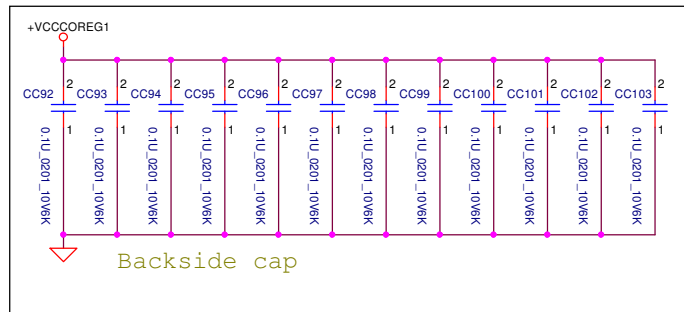
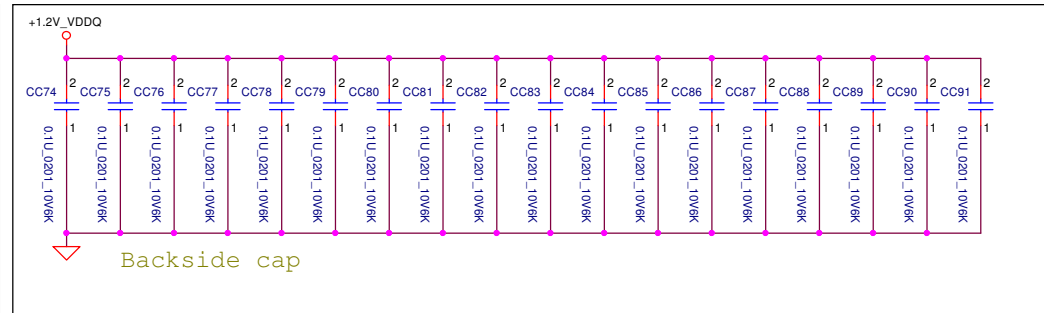
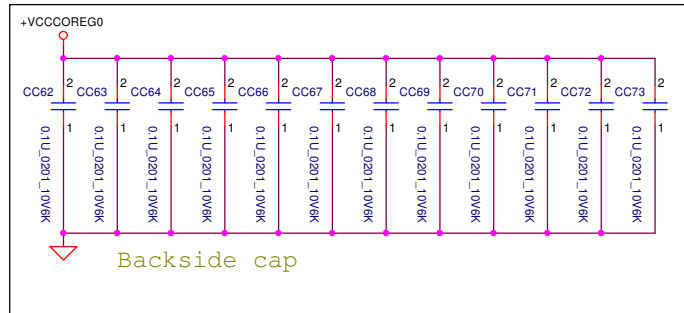


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(15) +VCCCOREG0  
(15) +VCCCOREG1  
(12,19,20,21,44) +1.2V\_VDDQ  
(5,12,47) +0.85VS\_VCCIO

○+VCCCOREG0  
○+VCCCOREG1  
○+1.2V\_VDDQ  
○+0.85VS\_VCCIO



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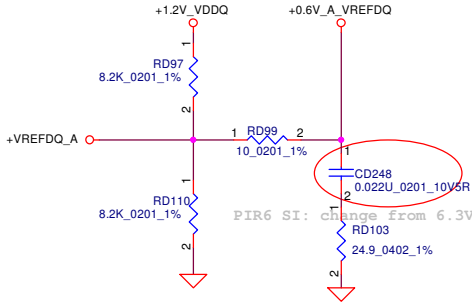
SKL Y-PROCESSOR DECOUPLING

Rev 0.1

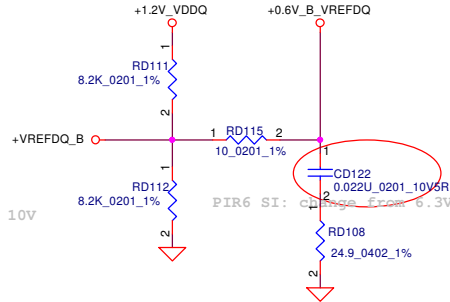




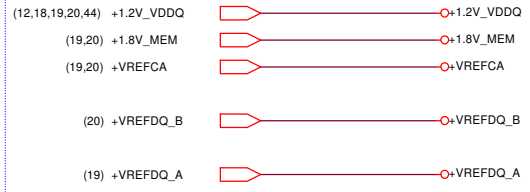
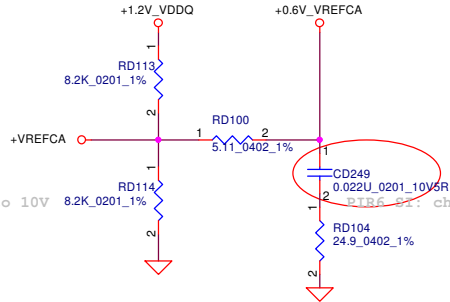
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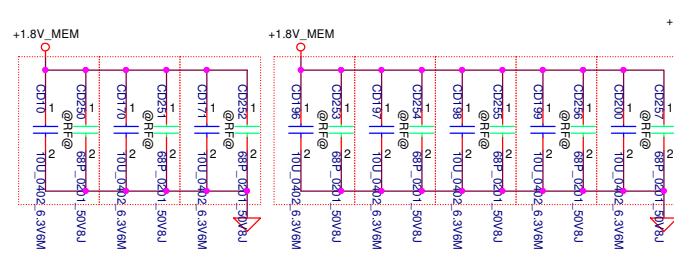
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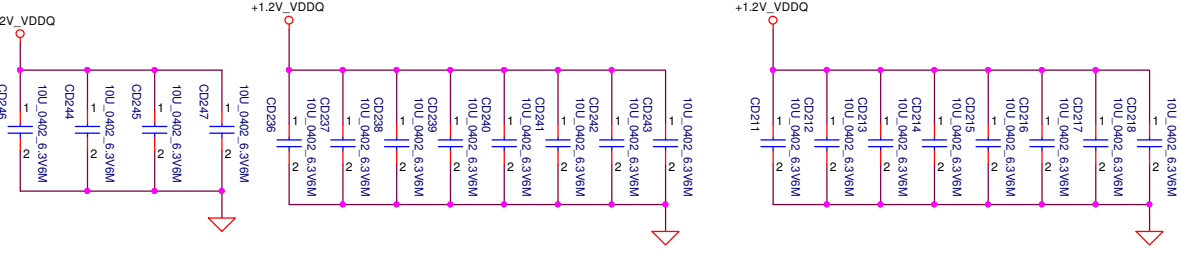
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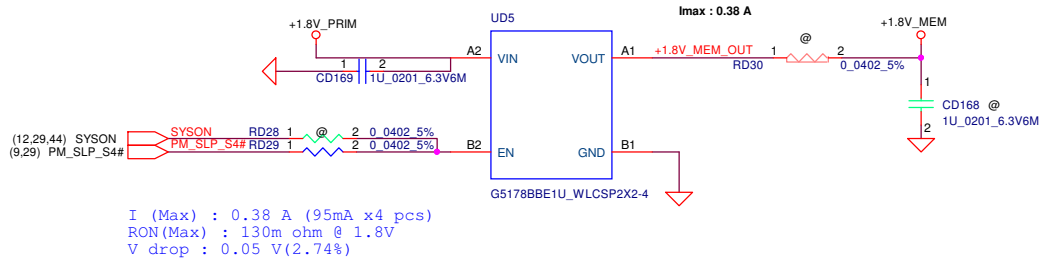
VDD1 DECAPS



VDDQ DECAPS

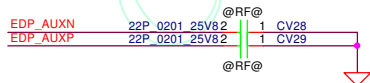
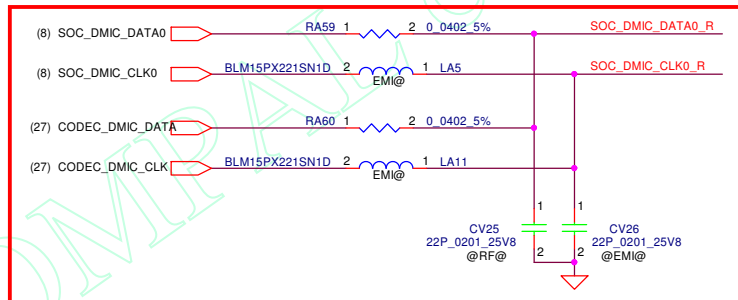
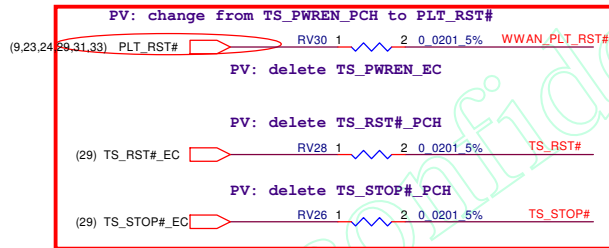
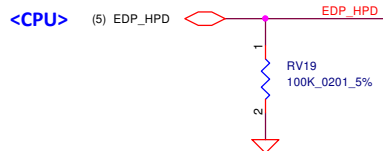
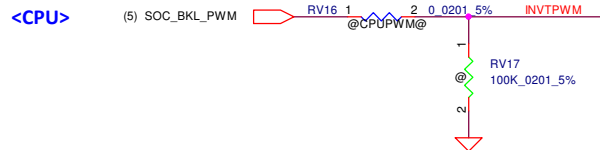
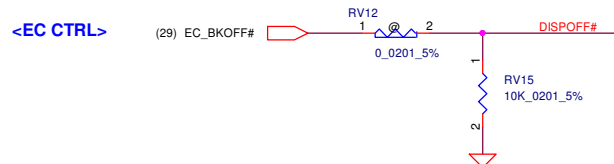
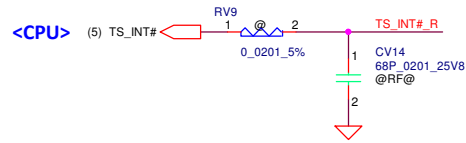


+1.8V\_PRIM TO +1.8V\_MEM



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					LPDDR3 VREF
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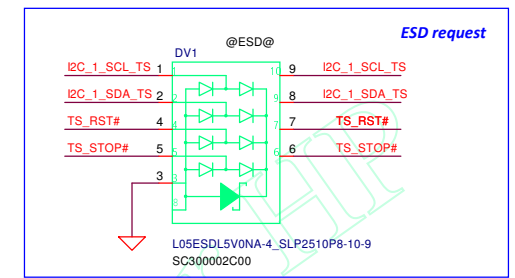
# eDP Control:1.2/4.12



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(27,29,30,39) +5VS

(5,7,9,10,11,24,27,29,31,36,37,39,47,48) +3VS



I (Max) : 2A

RON(Max) : 70m ohm

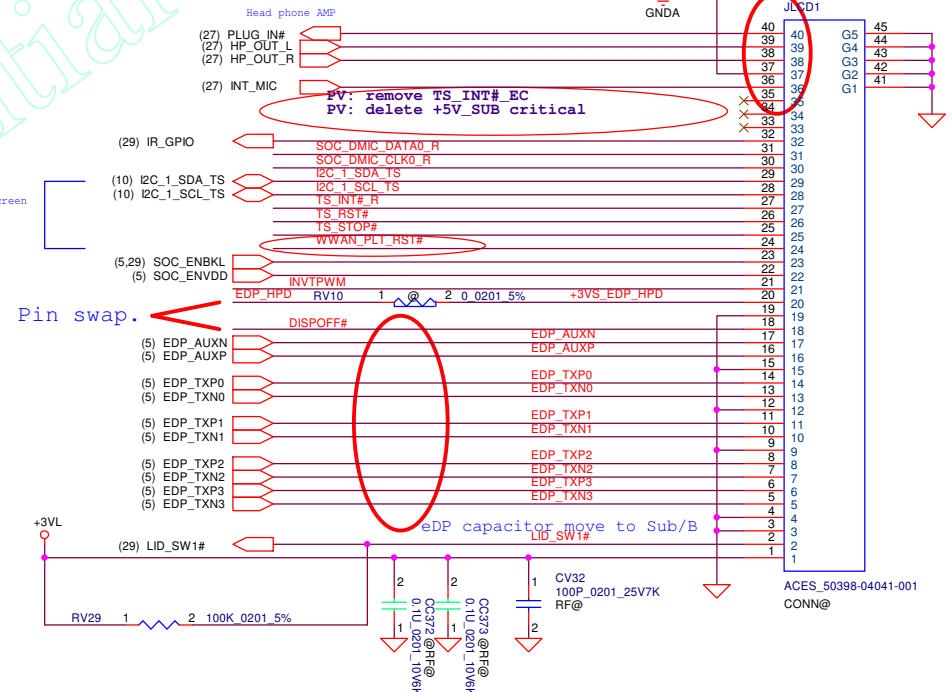
V drop : 0.14 V(=2.8%)

+5VALW TO +5VS\_SUB

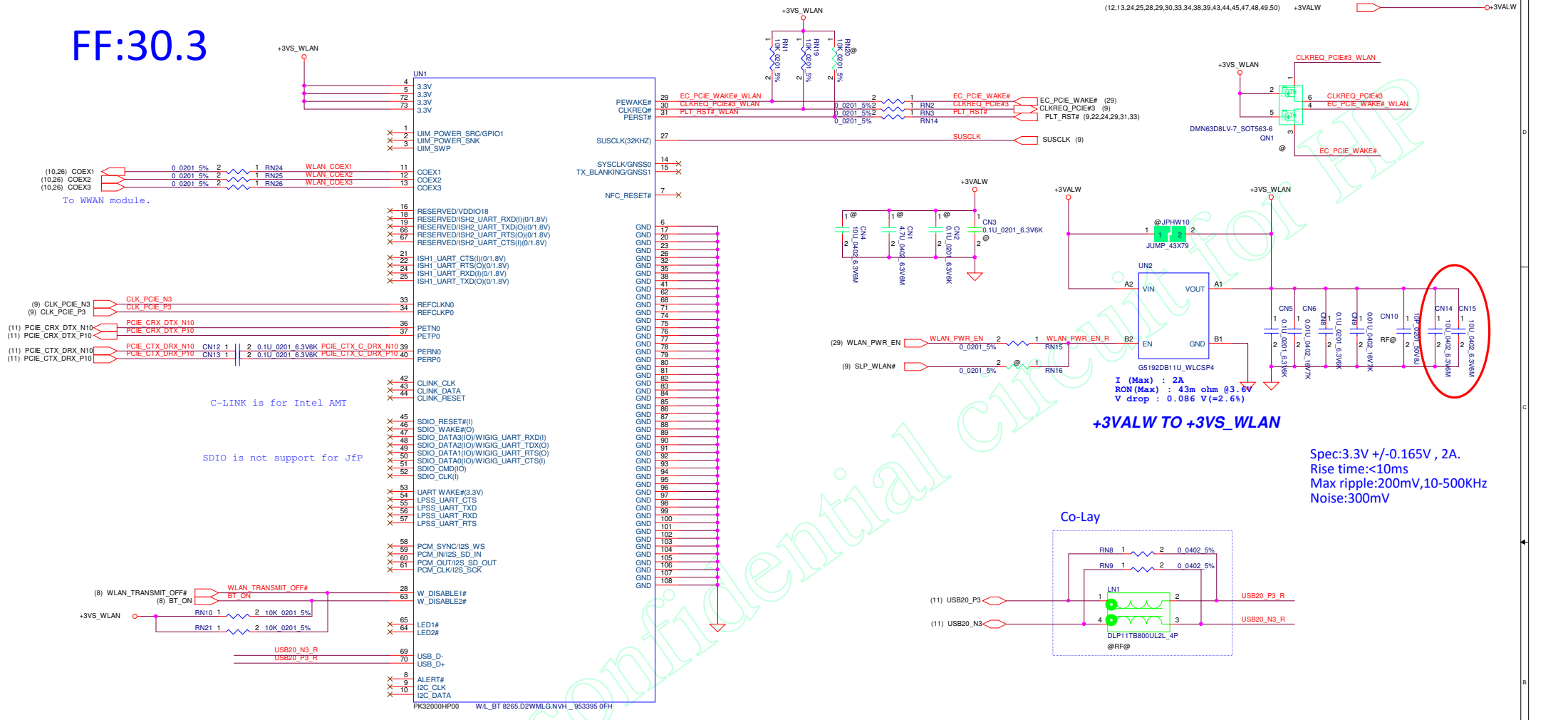
For IR camera & HP AMP

PIR38 SI: Remove +5VS\_SUB

PV: delete +5V\_SUB critical



# FF:30.3



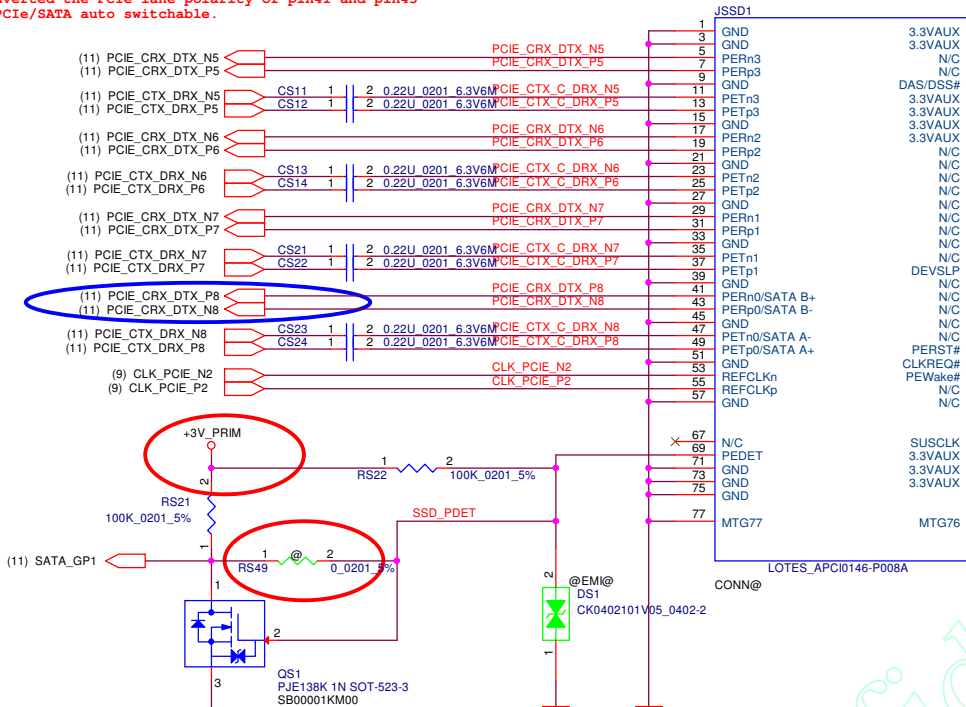
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(5,7,9,10,11,27,29,31,36,37,39,47,48) +3VS

+3VS

+3VS\_SSD

It inverted the PCIe lane polarity of pin41 and pin43 for PCIe/SATA auto switchable.



I (Max) : 3 A  
RON(Max) : 43m ohm @ 3.6V  
V drop : 0.129V (~3.9%)

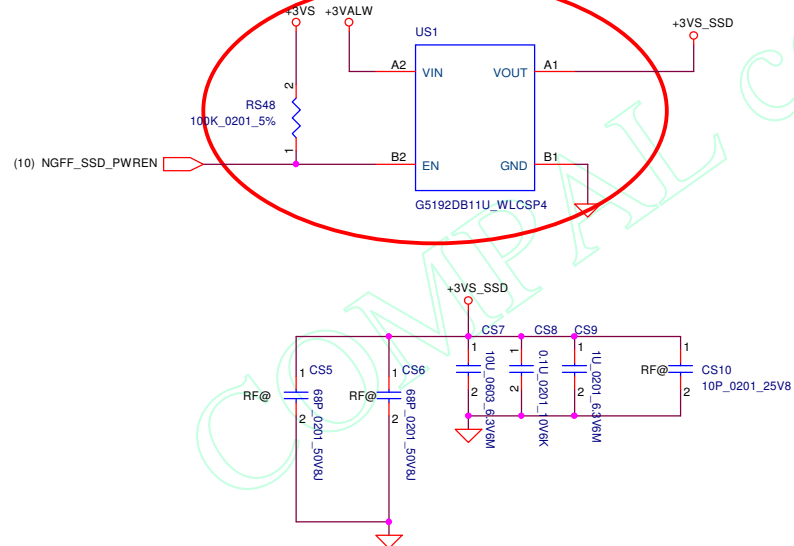
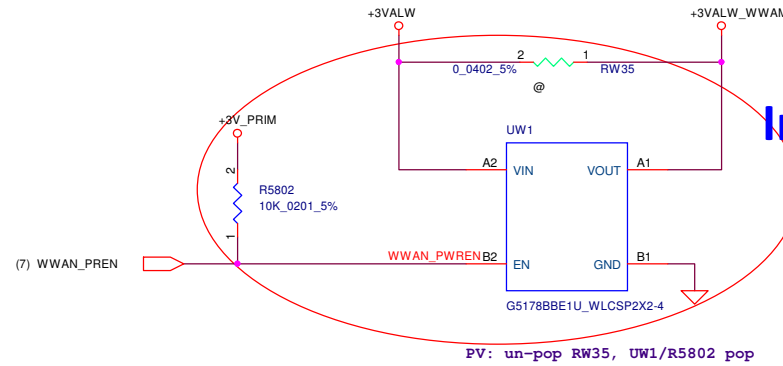


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

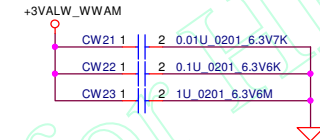
Pin	Signal	Signal	Pin
74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	Connector Key	67
58	N/C	Connector Key	
56	N/C	Connector Key	
54	PEWAKER (I/O)(0/3.3V) or N/C	Connector Key	
52	CLKREQ# (I/O)(0/3.3V) or N/C	Connector Key	
50	PERST# (O)(0/3.3V) or N/C	Connector Key	
48	N/C	GND	57
46	N/C	REFCLKp	55
44	N/C	REFCLKn	53
42	N/C	GND	51
40	N/C	PETp0/SATA-A+	49
38	DEVSLP (O)	PETn0/SATA-A-	47
36	N/C	GND	45
34	N/C	PERp0/SATA-B-	43
32	N/C	PERn0/SATA-B+	41
30	N/C	GND	39
28	N/C	PETp1	37
26	N/C	PETn1	35
24	N/C	GND	33
22	N/C	PERp1	31
20	N/C	PERn1	29
18	3.3V	GND	27
16	3.3V	PETp2	25
14	3.3V	PETn2	23
12	3.3V	GND	21
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	PERp2	19
8	N/C	PERn2	17
6	N/C	GND	15
4	3.3V	PETp3	13
2	3.3V	PETn3	11
		GND	9
		PERp3	7
		PERn3	5
		GND	3
		GND	1

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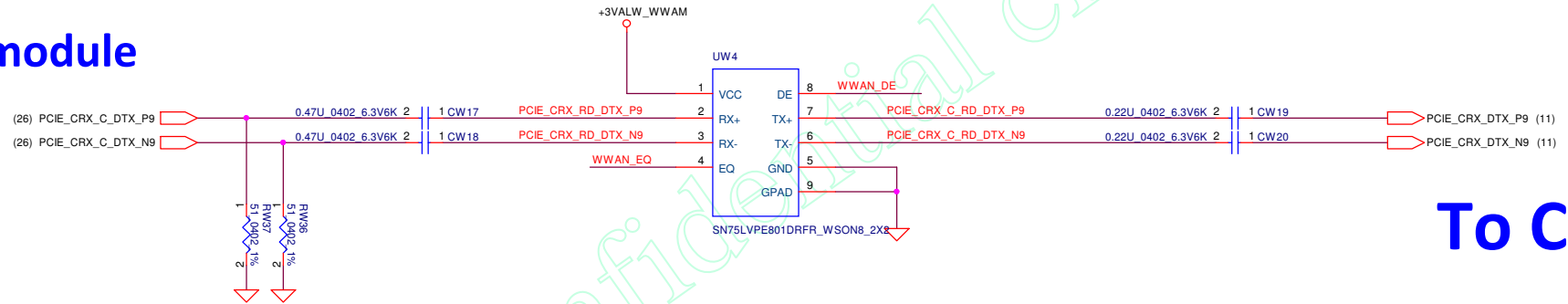
# FF:32.3



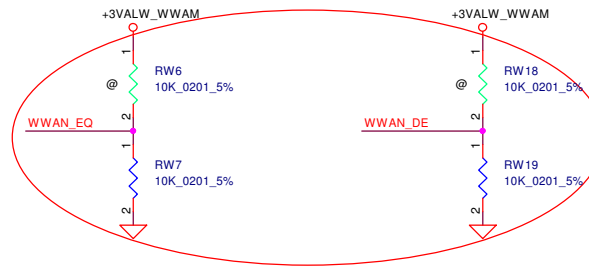
I (Max) : 0.04A  
 RON(Max) : 95m ohm @ 3.6V  
 V drop : 0.0038 V(=0.12%)



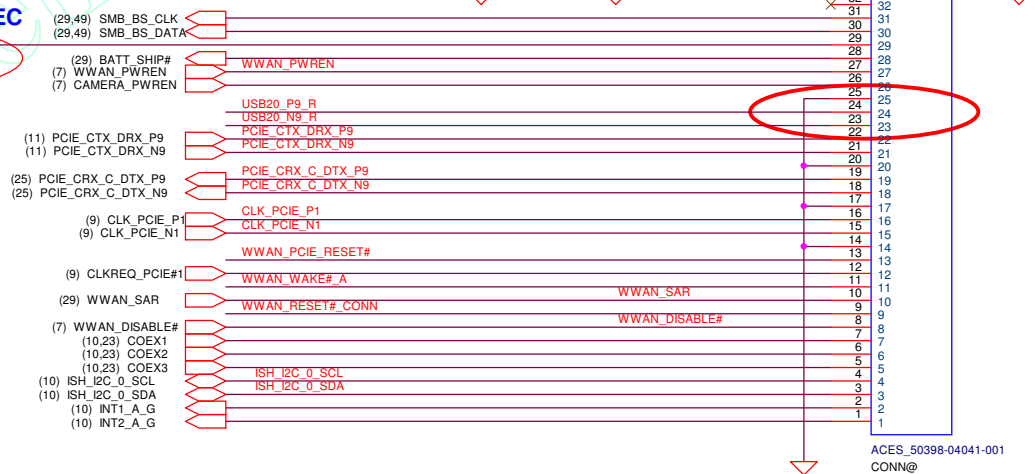
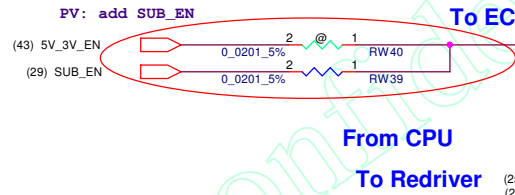
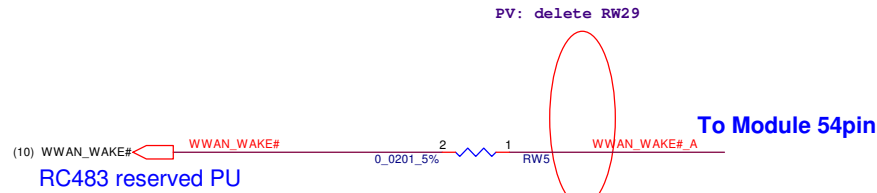
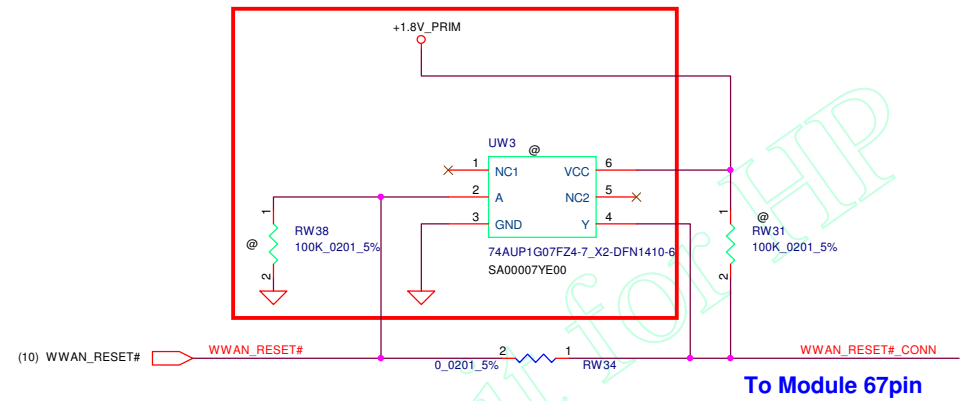
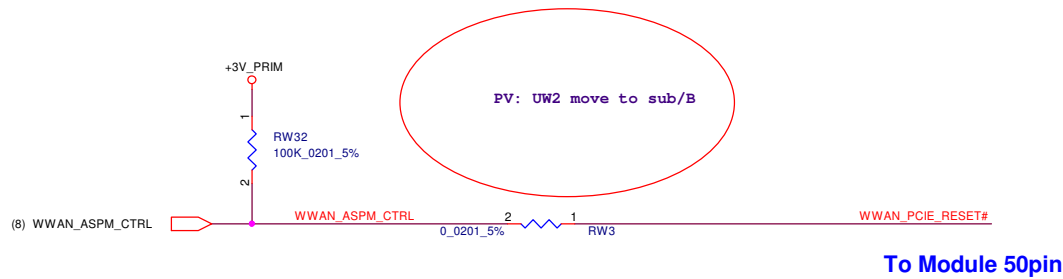
**From module**



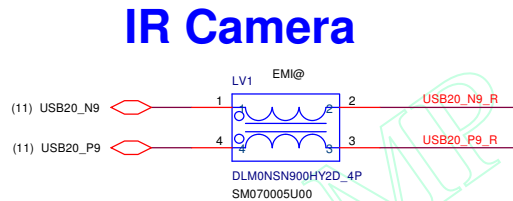
PIR5 SI: WWAN Pcie change EQ setting



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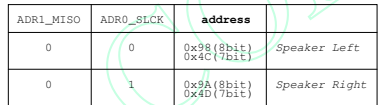
FF:32.3



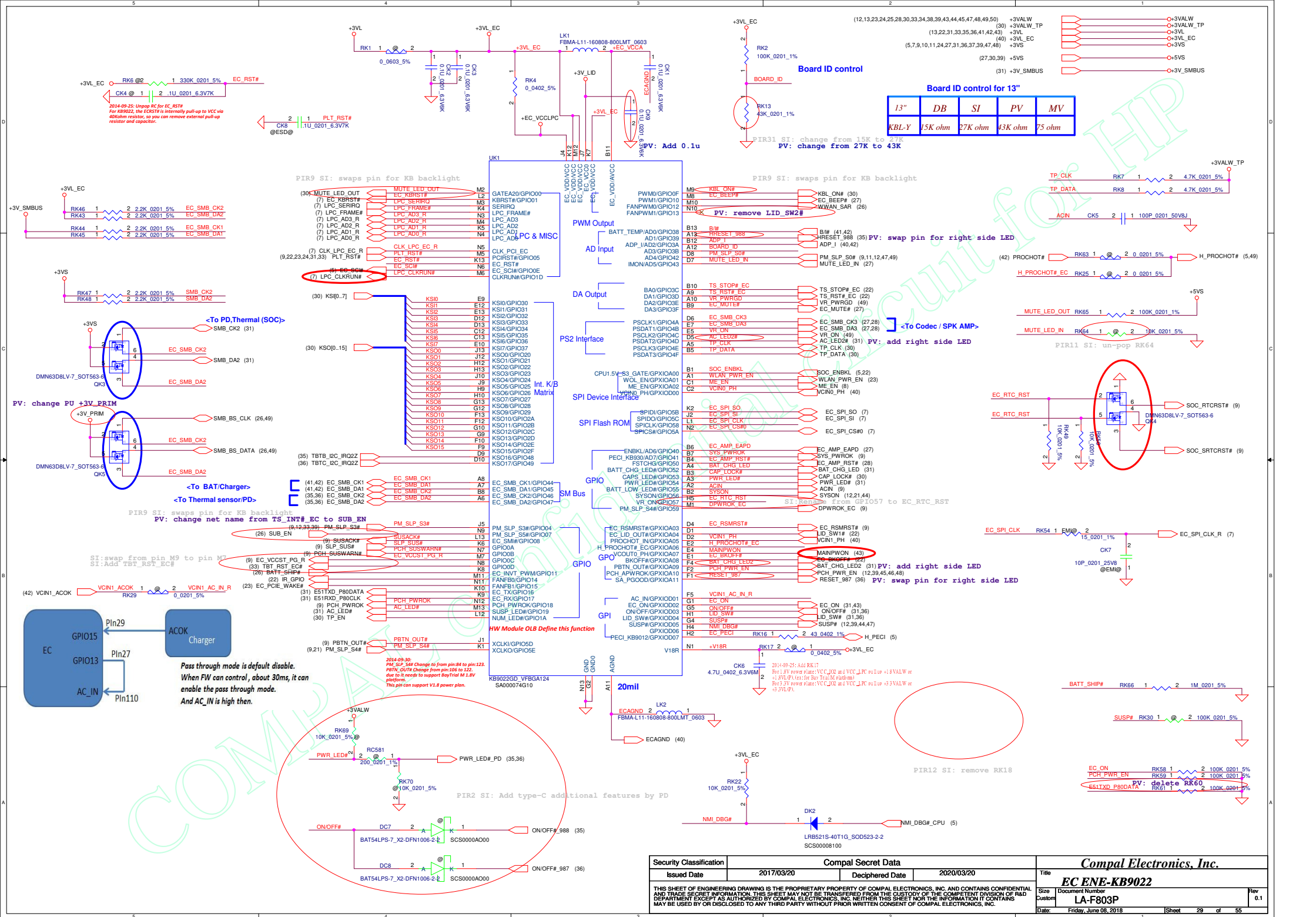
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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2020/03/20				Title				WWAN CONN			
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## IC:10.2

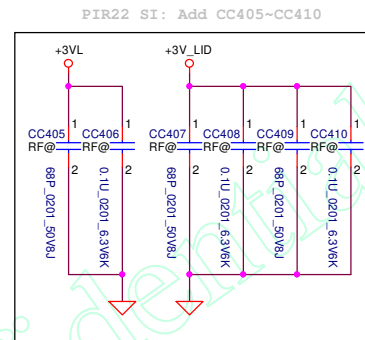
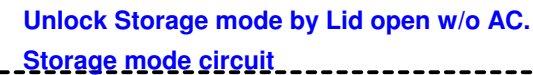


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<p>Doc Number</p> <p>LA-F803P</p> <p>Day: 08/08/2018</p>				Sheet	28 of 55





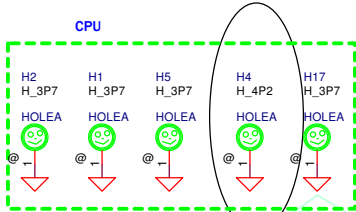
## Function Field:29.5



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				Date:	Friday, June 08, 2018	Sheet	31 of 55

Remove HP2DC

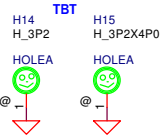
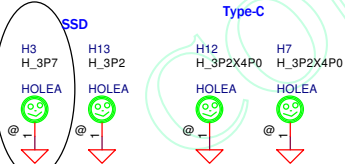
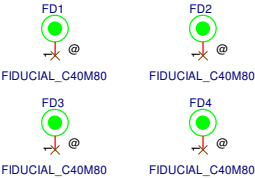
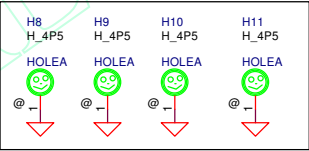
Screw Hole



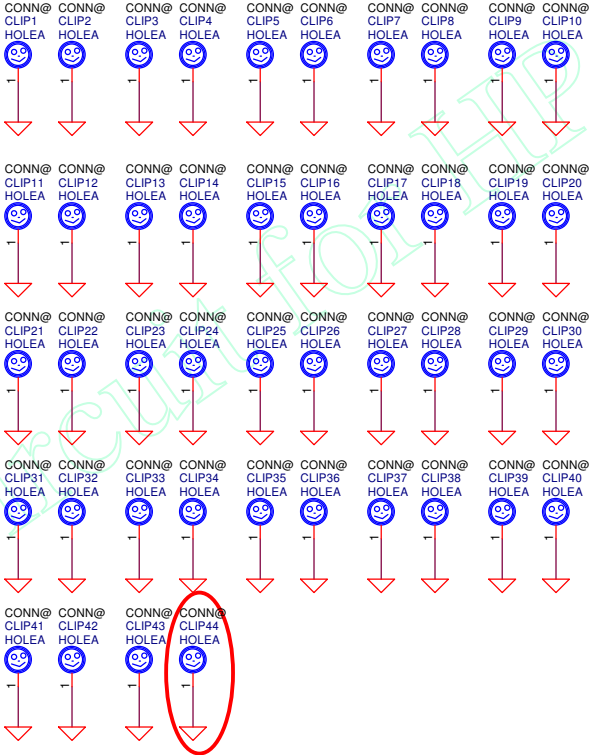
WLAN

HOLEA

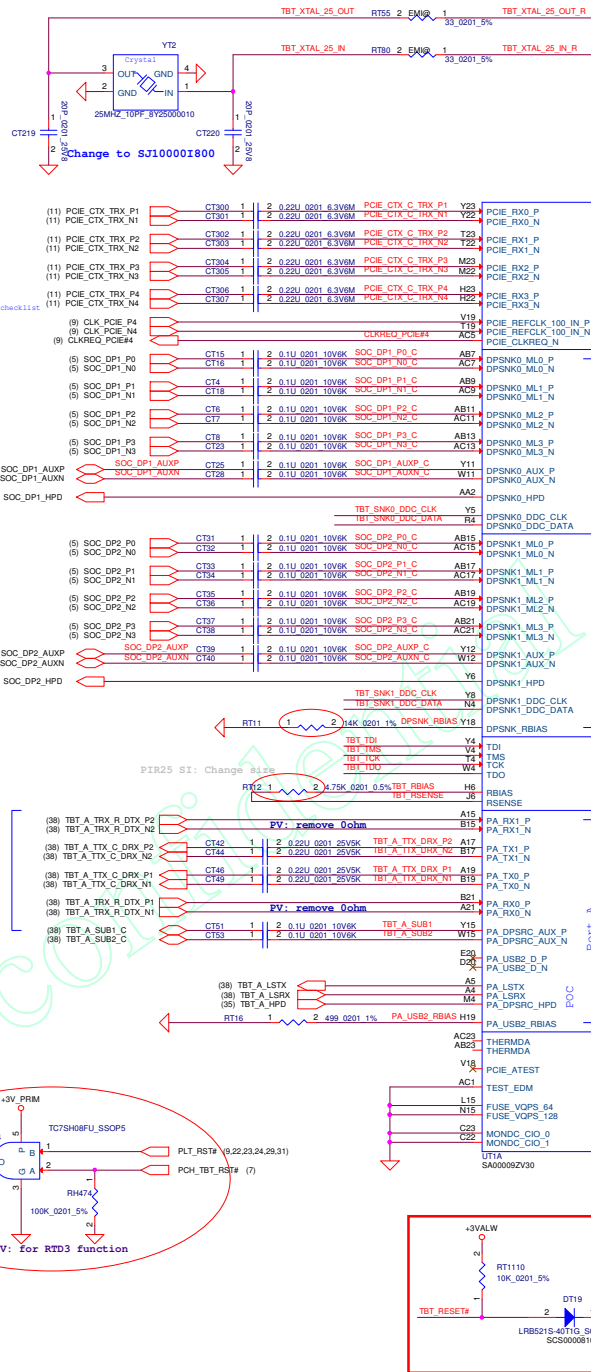
Hinge



Shielding Can Clip



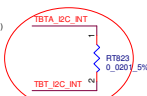
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## FF:46.2



For TUSB546A



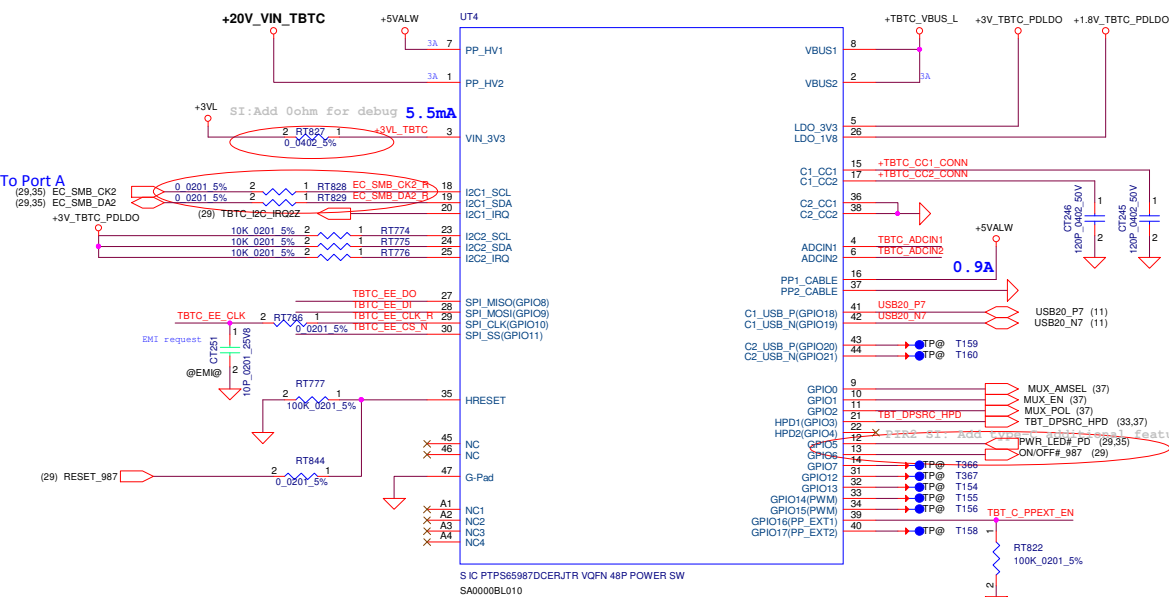
From TPS65988

JTYPEC1

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Date:	LA-F803P			Current:	1		
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To Port A

(29,35) EC\_SMB\_CK2

(29,35) EC\_SMB\_DA2

+3V\_TBTC\_PDLO

TBTC\_EE\_CLK

TBTC\_EE\_DI

TBTC\_EE\_CLK\_R

TBTC\_EE\_CS\_N

EM1 request

RT777

RT844

RESET\_987

NC

NC

NC

NC

NC

NC

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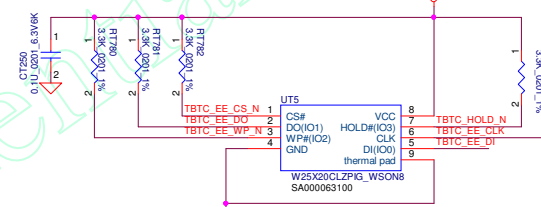
NC

Table 6. I<sup>2</sup>C Address Selection

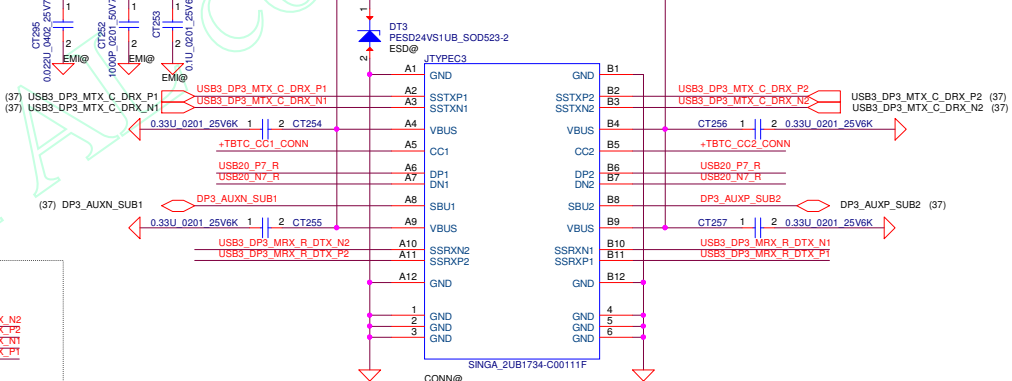
DIV = R2/(R1+R2) <sup>(1)</sup>		I <sup>2</sup> C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR_DECODE	
0.00	0.18	000b	
0.20	0.38	001b	
0.40	0.58	010b	
0.60	1.00	011b	

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

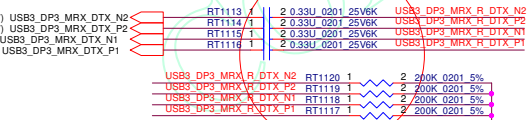
## SPI



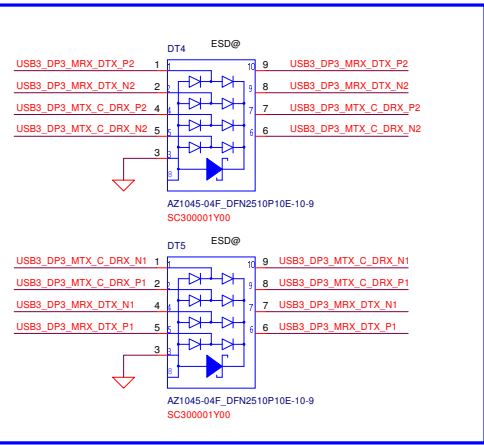
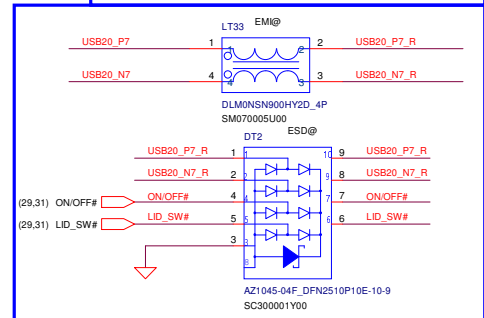
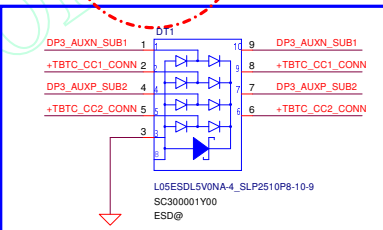
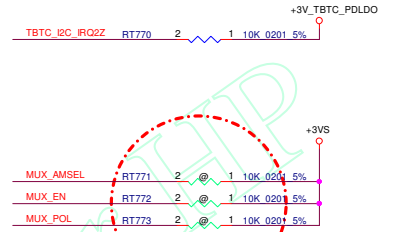
W = 200 mils



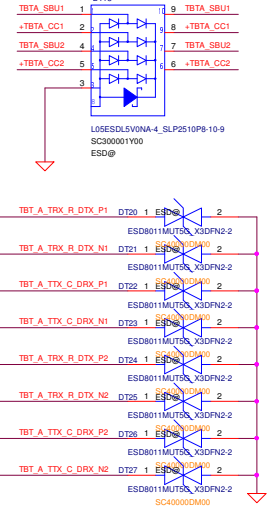
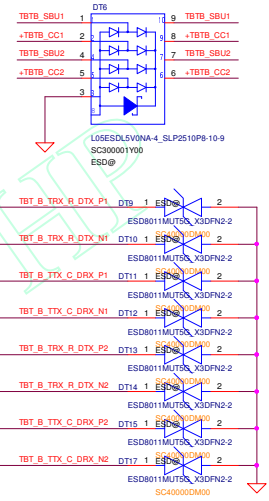
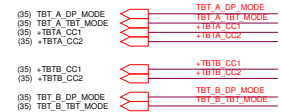
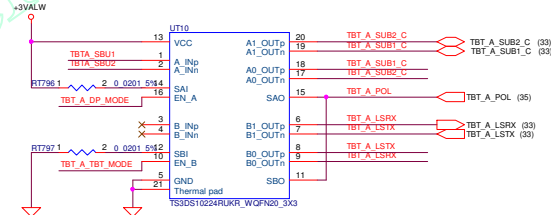
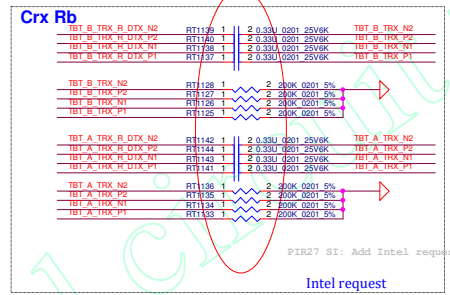
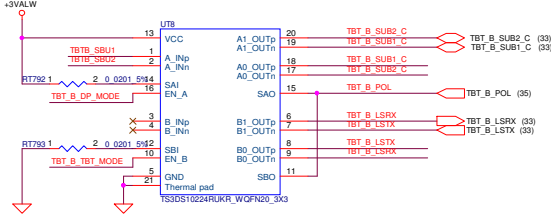
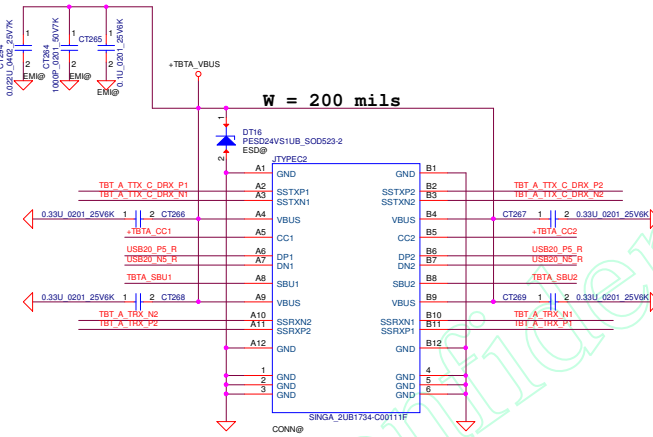
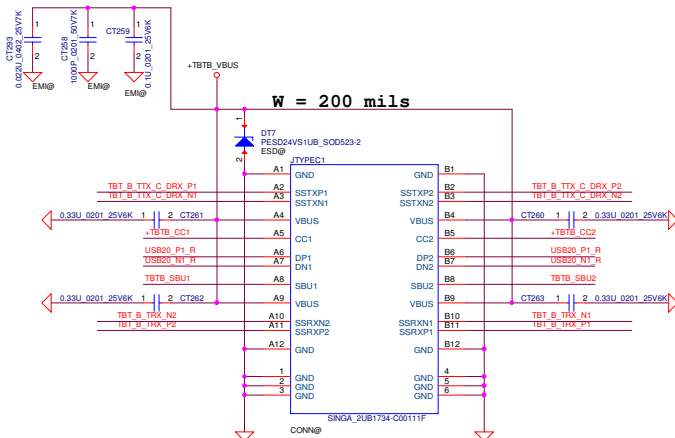
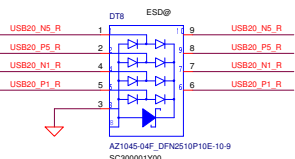
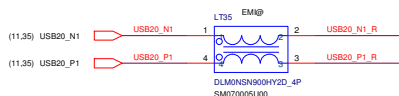
## Crx Rb



Intel request







TS3DS10224 Function Table

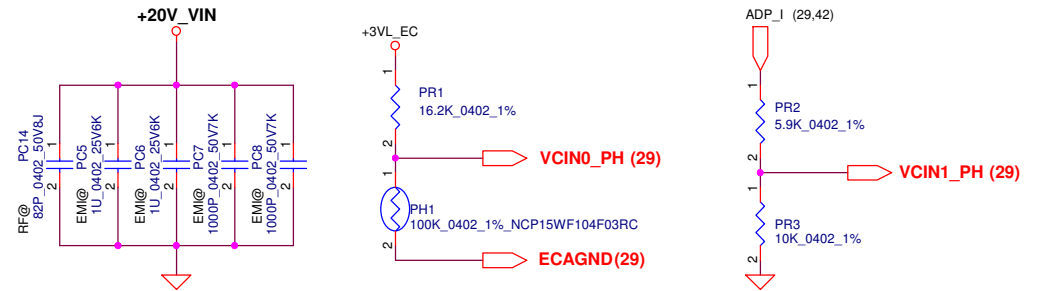
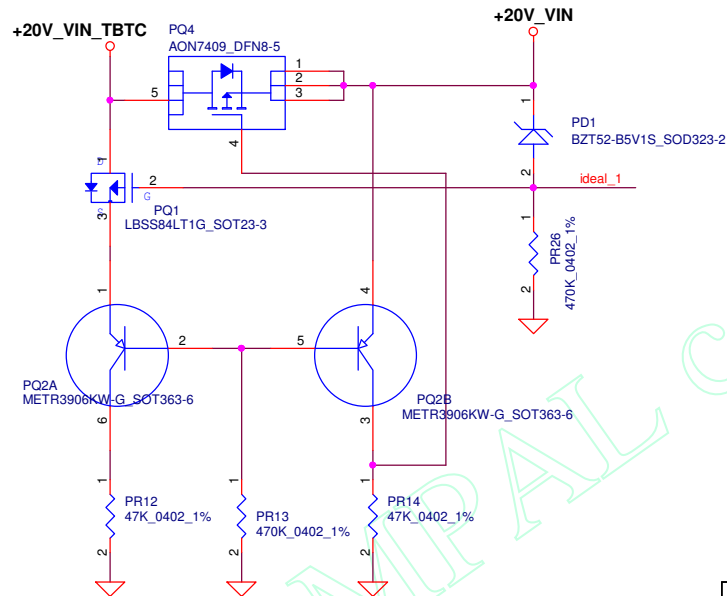
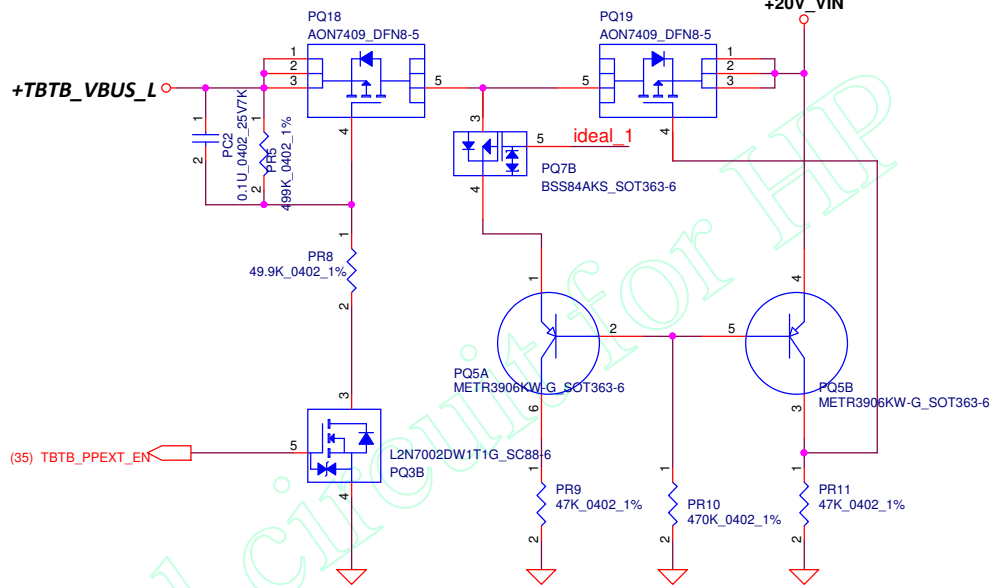
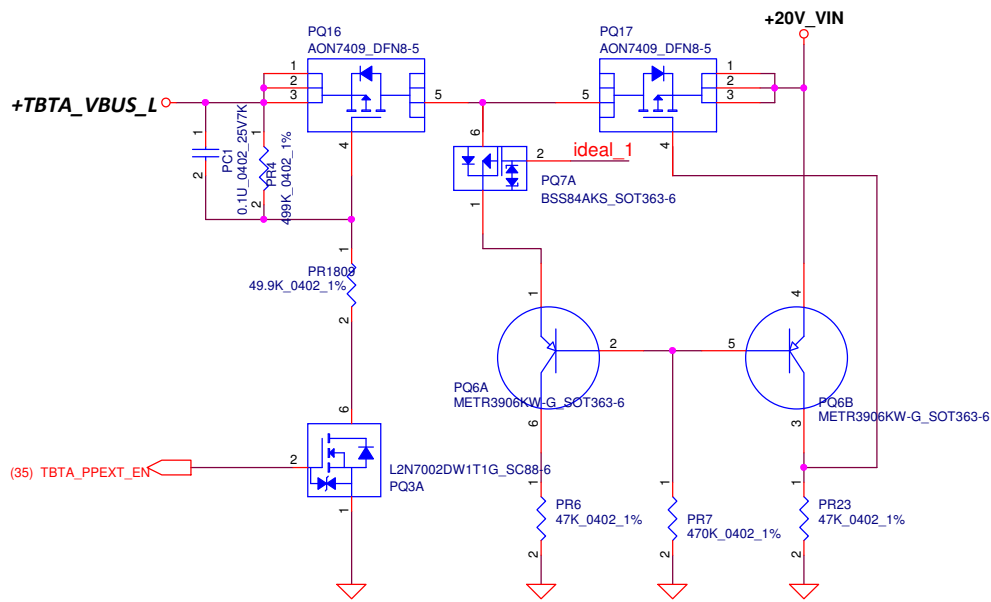
NX3DV221GM Function Table

SBU1	SBU2	(ENA)	(ENB)	(SAO/SBO)	OUTA0	OUTA1	OUTB0	OUTB1
Hi-Z	Hi-Z	0	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
AUX_P	AUX_N	1	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
AUX_N	AUX_P	1	0	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z
LSTX	LSRX	0	1	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
LSRX	LSTX	0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z

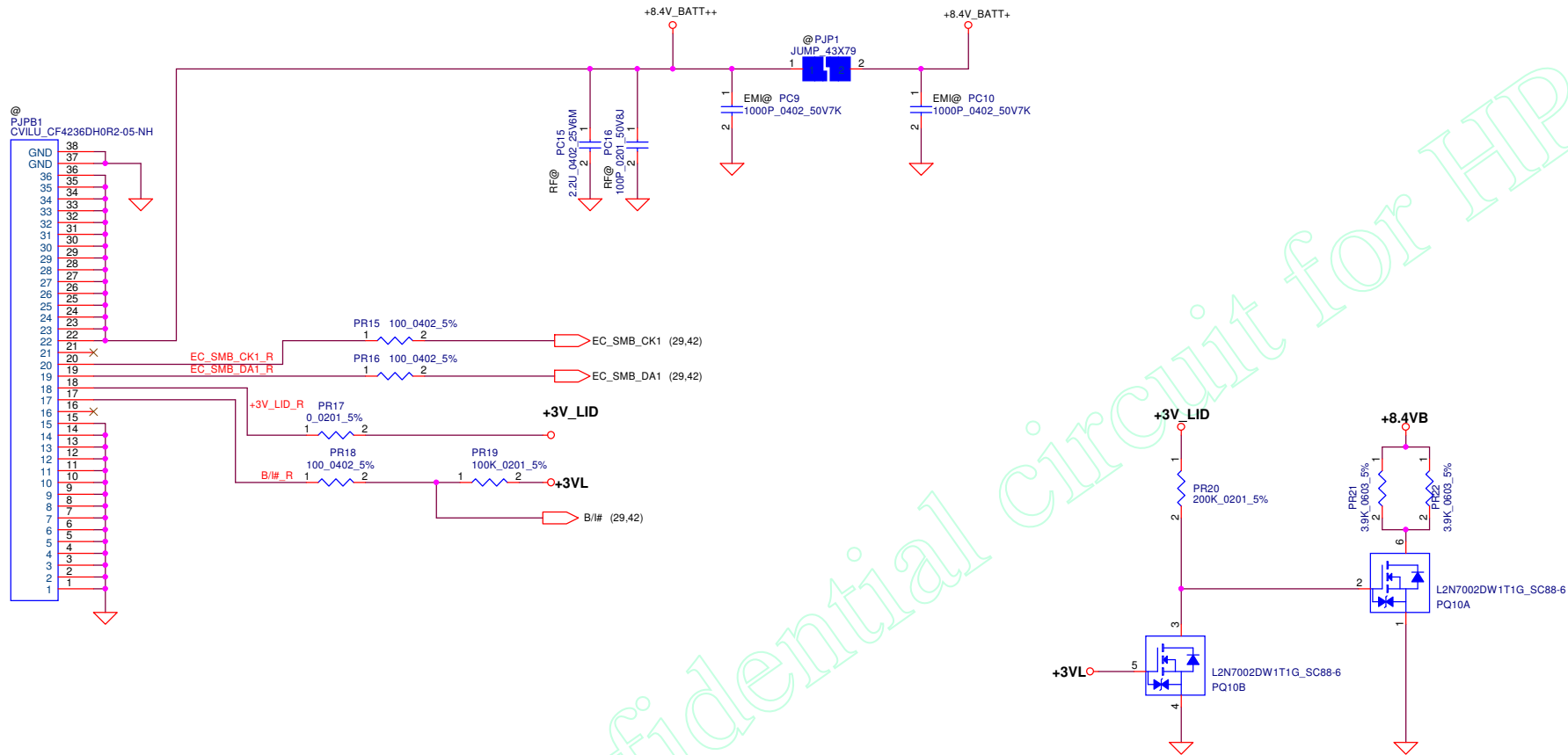
Input	OE	Channel
S	L	D+ = 1D+; D- = 1D-
L	L	D+ = 2D+; D- = 2D-
H	H	switches off

ENA	ENB	OUTA0	OUTA1	OUTB0	OUTB1
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	Hi-Z	EN	EN
1	0	EN	EN	Hi-Z	Hi-Z
1	1	EN	EN	EN	EN



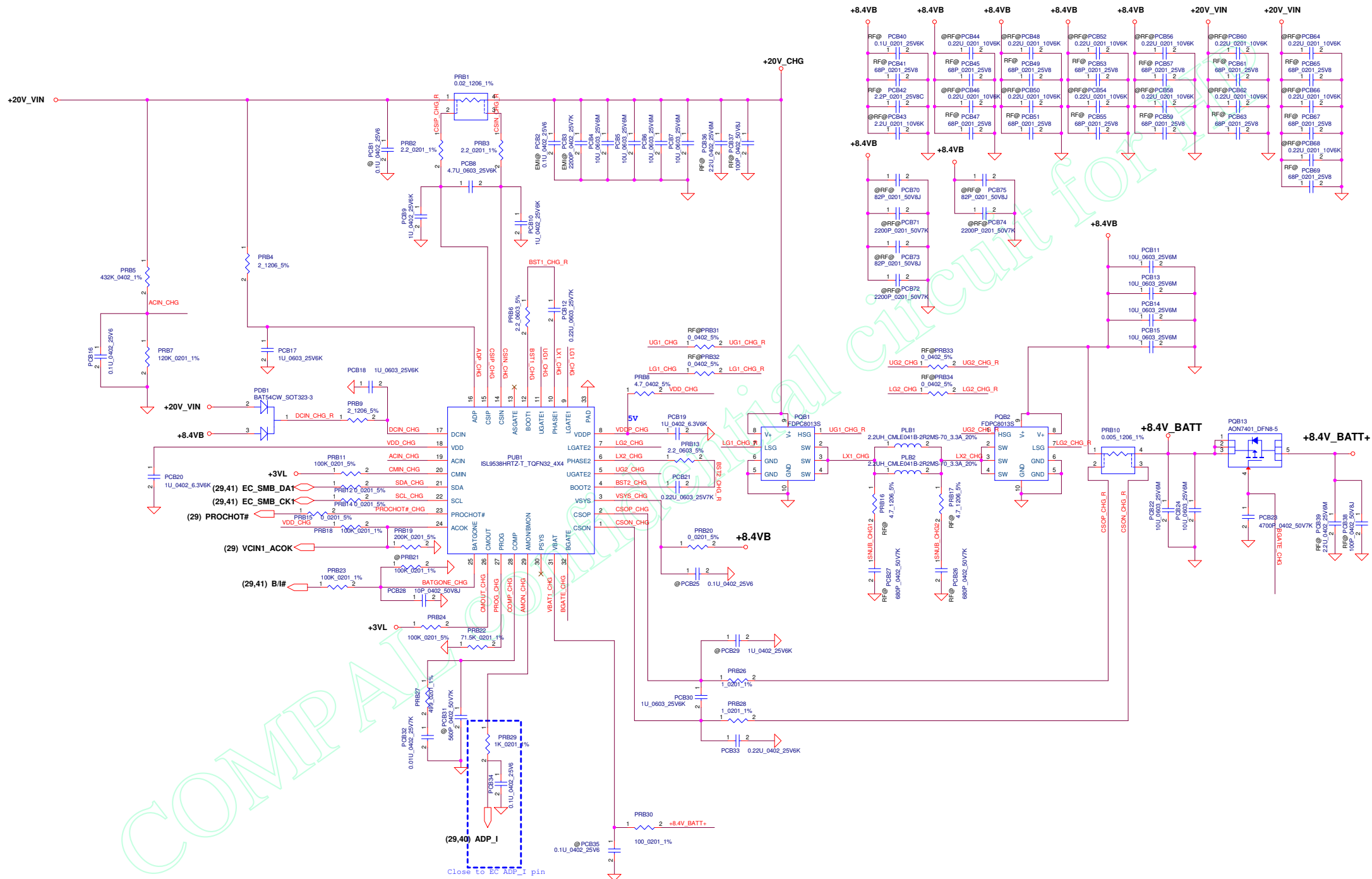


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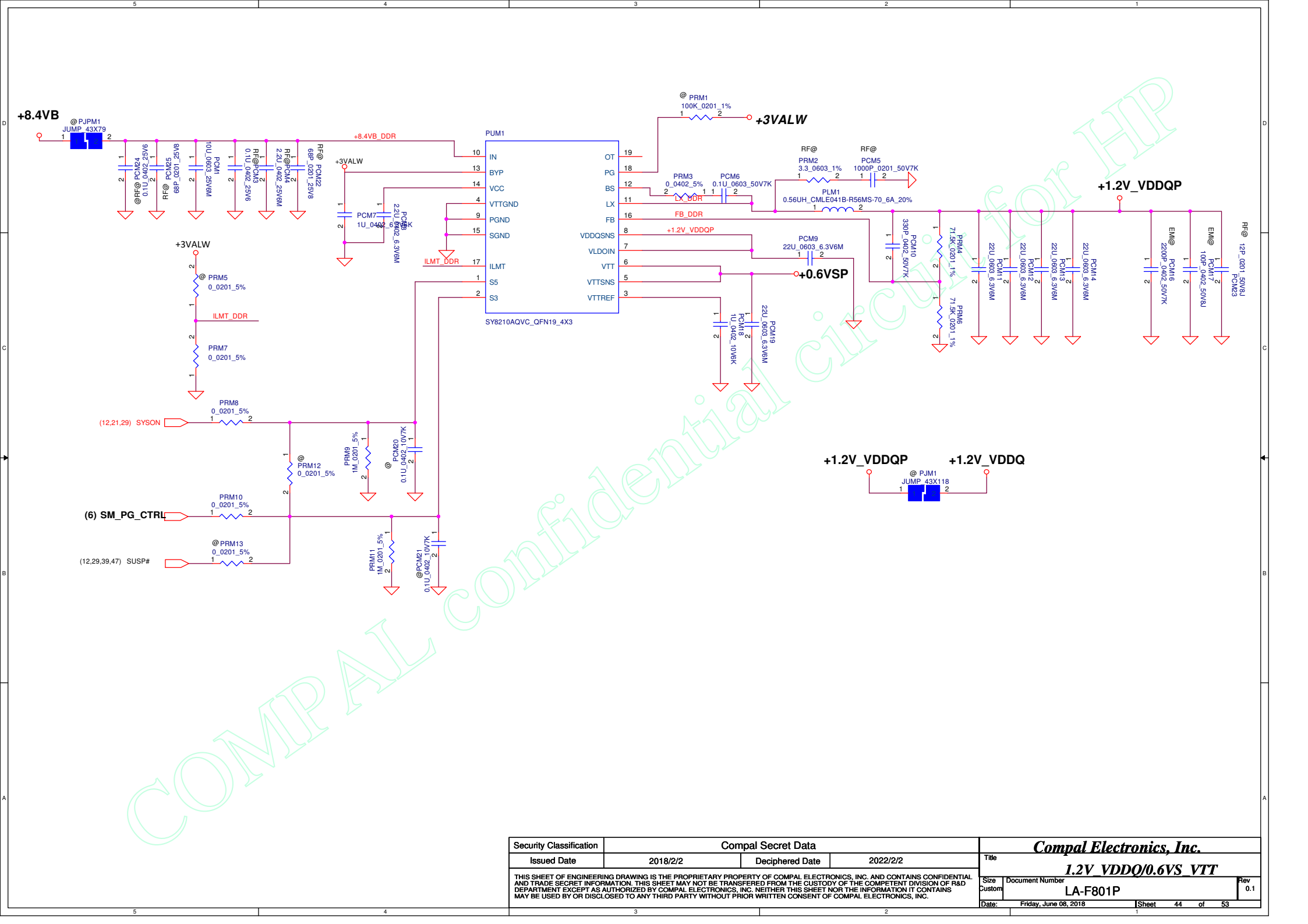
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★ can not stuff 10V rated MLCC

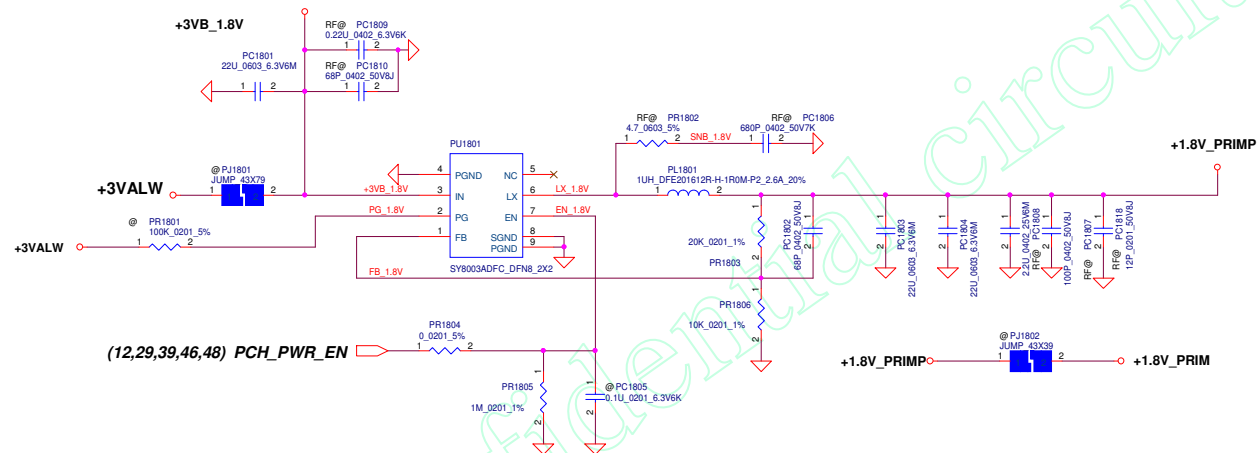


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+8.4VB

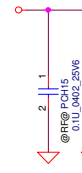
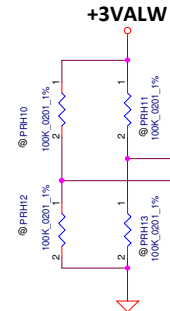
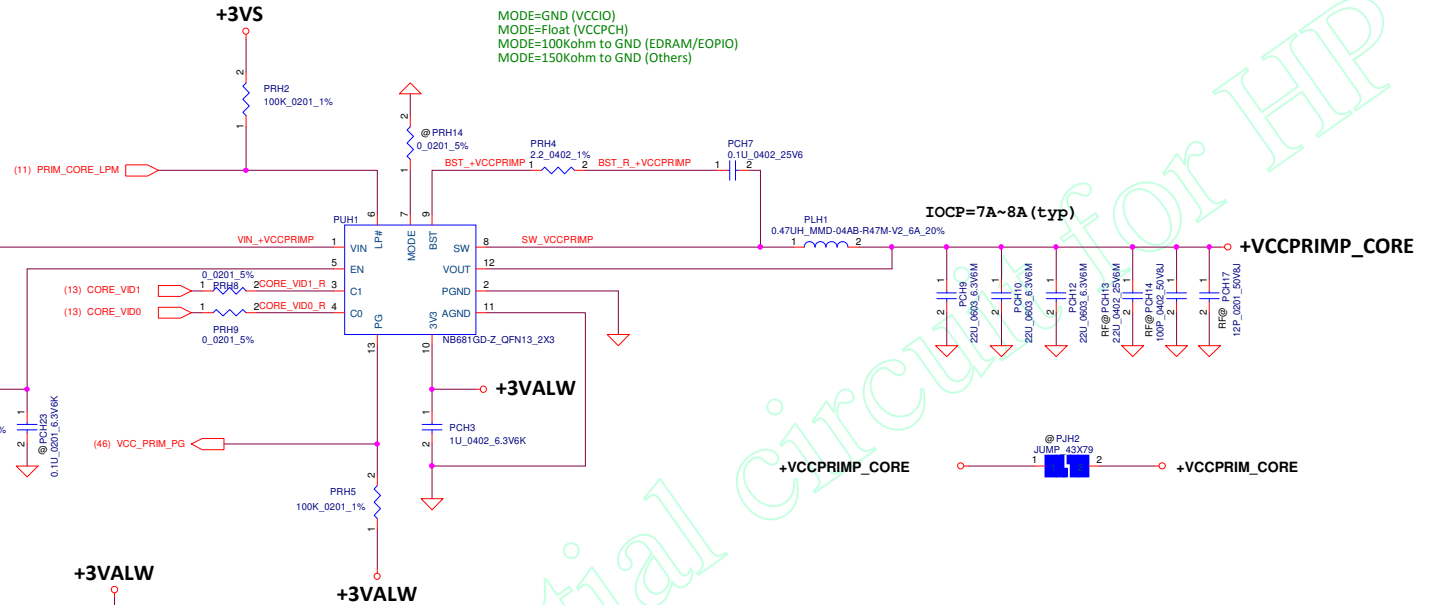
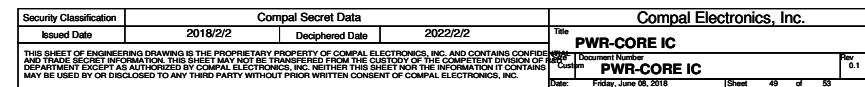


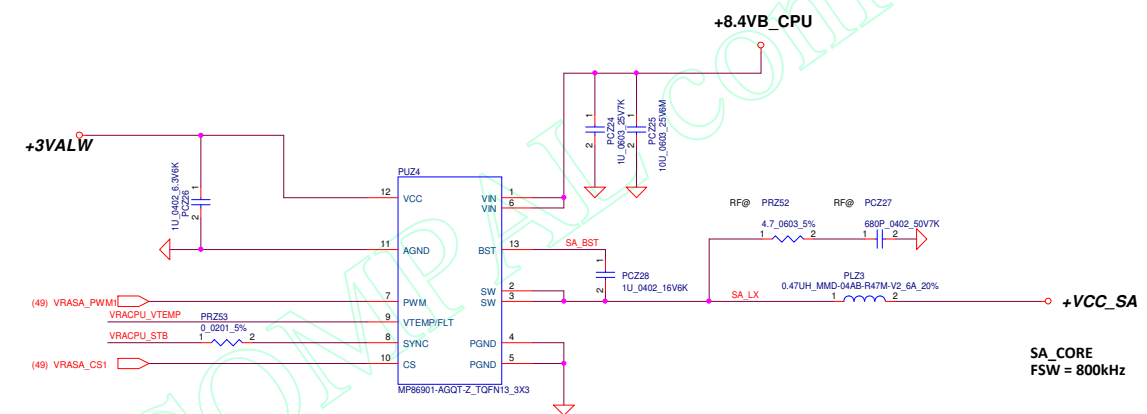
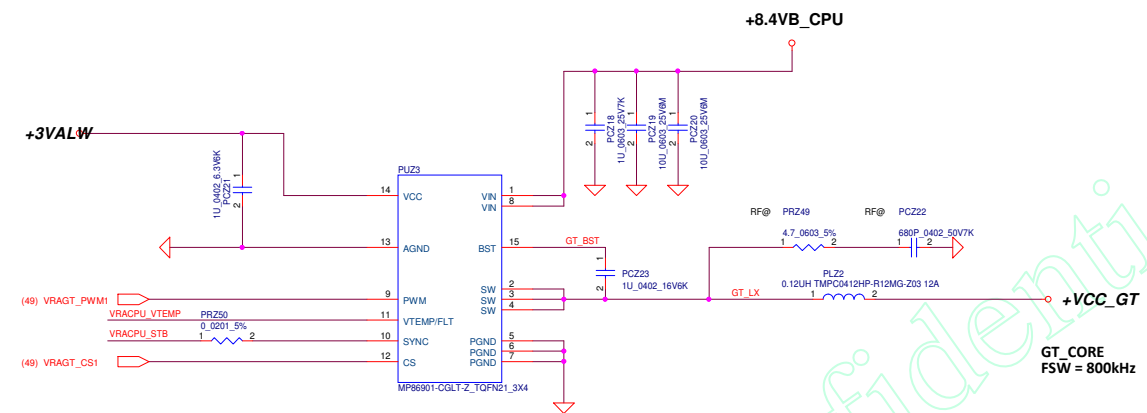
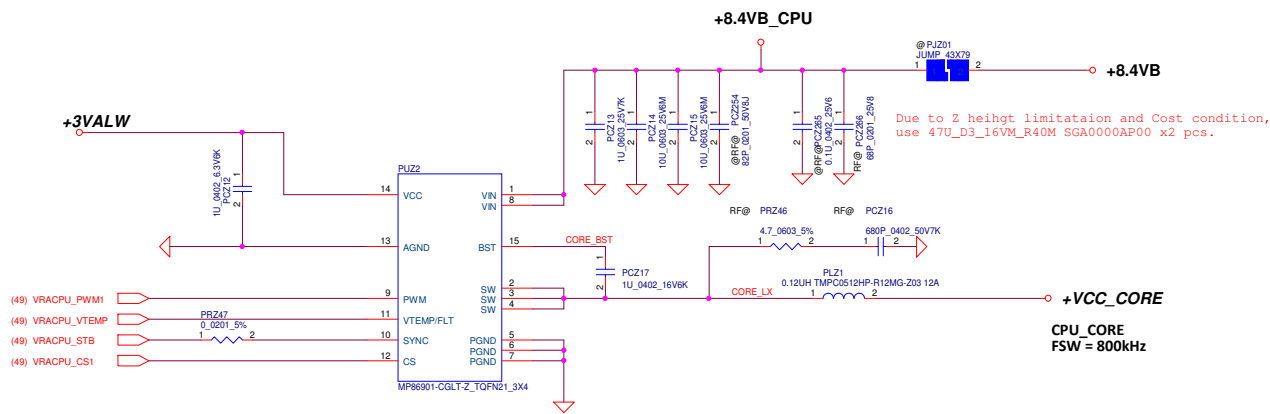
Table 3—Control Bit Definitions

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

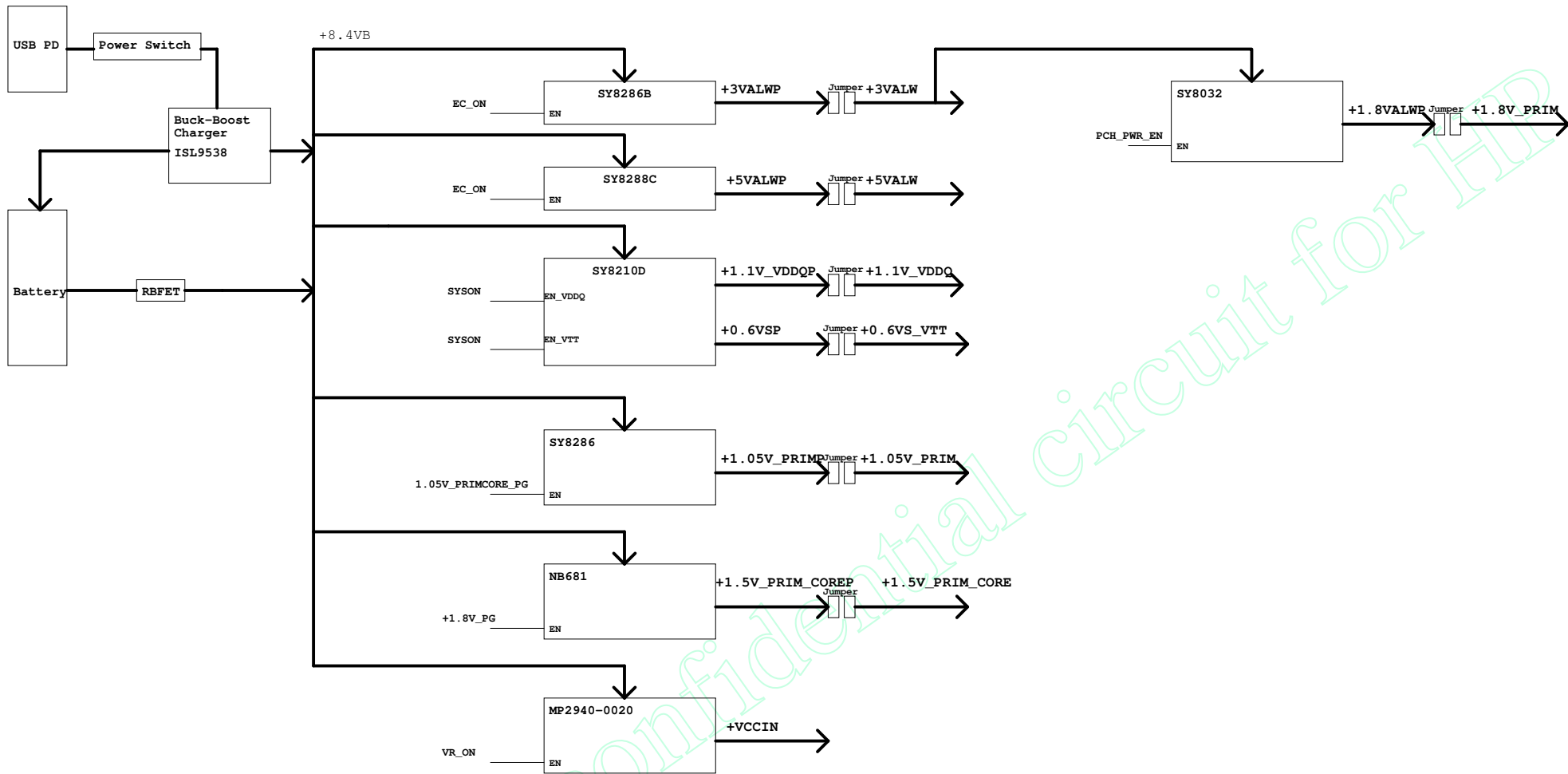


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PV Version change list (P.I.R. List)

Item	Date	Material	Reason For Change	Location	Phase
1	2018/05/30	S RES 1/16W 3.16K +-1% 0402 to S RES 1/16W 3.65K +-1% 0402	FAE recommend for KBL Y	PRZ34	PV
2	2018/05/30	S RES 1/20W 133K +-1% 0201 to S RES 1/20W 154K +-1% 0201	FAE recommend for KBL Y	PRZ38	PV
3	2018/05/30	S RES 1/10W 4.7 +-5% 0603 to S RES 1/10W 3.3 +-1% 0603	RF MLCC shortage lead to change	PRM2 · PR314	PV
4	2018/05/30	S CER CAP 680P 50V K X7R 0201 to S CER CAP 1000P 50V K X7R 0201	RF MLCC shortage lead to change	PC337,PCM5	PV
5	2018/05/30	S RES 1/20W 100K +-1% 0201to S RES 1/20W 71.5K +-1% 0201	shortage	PRM4,PRM6	PV
6	2018/05/30	S CER CAP .1U 16V K X7R 0603 to S CER CAP 0.1U 50V K X7R 0603	shortage	PCM6	PV
7	2018/05/30	S CER CAP 4700P 25V K X7R 0402 to S CER CAP 4700P 50V K X7R 0402	shortage	PCB23	PV
8	2018/05/30	S CER CAP 12P 25V J NPO 0201 to S CER CAP 12P 50V J NPO 0201	shortage	PC342,PC343,PC1015,PC1818,PCH17,PCM23,PCZ264	PV
9	2018/05/30	S CER CAP 220P 25V K NPO 0402 to S CER CAP 220P 50V J NPO 0402	shortage	PCZ8,PCZ9	PV
10	2018/05/30	Delete S RES 1/20W 0 +-5% 0201	KBL_YRefresh	PRI3	PV
11	2018/05/30	S CER CAP 2200P 50V K X7R 0201to S CER CAP 0.047U 10V K X5R 0201	shortage	PCZ158,PCZ208,PCZ210,PCZ212,PCZ214	PV
12	2018/05/30	S CER CAP 82P 50V J NPO 0201 to S CER CAP 68P 25V J NPO 0201	shortage	PC339,PC341,PC1014,PCB41,PCB45,PCB47,PCB49,PCB51, PCB53,PCB55,PCB57,PCB59,PCB61,PCB63,PCB65,PCB67, PCB69,PCH16,PCI14,PCM22,PCM25,PCZ266	PV
13	2018/05/31	S RES 1/20W 0 +-5% 0201 to S RES 1/20W 20K +-1% 0201	KBL_YRefresh	PRI2	PV
14	2018/05/31	add S RES 1/16W 6.8 +-5% 0402,S RES 1/20W 0 +-5% 0201	local sense to remote sense	PRI9,PRI10,PRI11,PRI12	PV
15	2018/06/04	S CER CAP 100P 50V J NPO 0402 to S CER CAP 100P 50V J NPO 0201	connetor bigger	PC16	PV
16	2018/06/07	1U 6.3V K X5R 0402 to 1U 6.3V M X5R 0201	shortage	PCZ156,PCZ223,PCZ224	PV
17					
21					
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	10	PM_BATLOW# Add 10K PU	18/3/16	HW	Add RC580 10Kohm PU to +3VALW_DSW		0.2
2	29,35,36	PM_BATLOW# Add 10K PU	18/3/16	HW	Add type-C additional features		0.2
3	31	change R38 From 560 to 1.91K	18/3/22	HW	change R30 From SD034130180 to SD000000R580		0.2
4	30	change R30 From 1.3K to 1.8K	18/3/22	HW	change R38 From SD028560080 to SD0000009080		0.2
5	25	WWAN Pcie change EQ setting	18/3/22	HW	un-pop RW6,RW18 & pop RW7,RW19		0.2
6	21	change CD122,CD248,CD249 from 6.3V to 10V	18/3/22	HW	change from SE000006E00 to SE000007H00		0.2
7	13	change LC3 & L24 PN	18/3/22	HW	change from SMO1000BC00 to SMO1000NY00		0.2
8	12,18	change CC117 & C5245 PN	18/3/23	HW	change from SE000000K80 to SE000000QL10		0.2
9	29	EC swaps pin for KB backlight	18/3/28	HW	KBL_ON# change to M9 MUTE_LED_OUT change to M2 TS_INT#_EC change to N9		0.2
10	11	For Port 3 USB2.0 function	18/4/3	HW	pop RH125		0.2
11	29	For KB mute LED function	18/4/3	HW	un-pop RK64		0.2
12	29	HW Design change	18/4/3	HW	remove RK18		0.2
13	28	RF request	18/4/10	RF	remove CA98,CA99		0.2
14	26	ESD request	18/4/10	ESD	remove D6		
15	27	ESD request	18/4/10	ESD	remove DA10,DA11		
16	28	ESD request	18/4/10	ESD	remove DA6,DA9		
17	28	HW Design change	18/4/11	HW	pop RA48		
18	18	RF request	18/4/16	RF	Add CC400-CC404		
19	18	RF request	18/4/16	RF	pop more Cap		
20	13	RF request	18/4/16	RF	remove CA98,CA99		
21	14	HW Design change	18/4/16	HW	un-pop RC147,RC148		
22	31	RF request	18/4/16	RF	Add CC405-CC410		
23	39	RF request	18/4/18	RF	Add -CC411-CC425		
24	7	Change UC2 to 16M	18/4/18	HW	Change from SA000051950 to SA00007XA10		
25	33	Change RT12 size	18/4/19	HW	Change from (0402) SD000011980 to (0201) SD0000024G00		
26	11	HW Design change	18/4/19	HW	pop UH3 , un-pop RC579		
27	38	Intel request	18/4/19	HW	By USB3.1 Type-C USB-IF ECN		
28	36	Intel request	18/4/19	HW	By USB3.1 Type-C USB-IF ECN		
29	39	RF request	18/4/19	RF	pop CH47		
30	39	RF request	18/4/19	RF	pop CC387,CC388		
31	29	Change board ID	18/4/20	HW	change from15K to 27K		

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